Seven stories from seven years of PULP project

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The PULP project in a nutshell

- Started in 2013, by Prof. Luca Benini
- We wanted to design energy efficient computing systems
  - Equally efficient for IoT and HPC over a wide range
- Key points
  - Parallel processing
  - Near threshold computing
  - Efficient switching between operating modes
  - Making best use of technology
  - Heterogeneous acceleration
Who is behind PULP?

Prof. Luca Benini

- Chief Architect in STMicroelectronics (2009-2012)
- h-index of 105 (June 2020), more than 49'000 citations, more than 1'000 publications
- 2016 IEEE CAS Mac Van Valkenburg award for sustained contributions on the design of energy-efficient ICs
- 2019 IEEE CEDA Donald O. Pederson award for work on Machine Learning acceleration
- Chief Architect in STMicroelectronics (2009-2012)

Frank Davide Rossi

- In total about 60 people work on projects related to PULP in Zurich and Bologna
  https://pulp-platform.org/team.html

ETH Zürich
- Leading Swiss Technical University
- Consistently ranks in the top 20 of the world
- 21'400 students
- 21 Nobel prizes

University of Bologna
- Founded in 1088, oldest university in the world
- More than 85'000 students
- One of the top ranked Universities in Italy and Europe

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Why Open Source Hardware

- **It is a necessity**
  - We can not afford to make everything ourselves, we need to collaborate
  - Makes it possible to work together quickly
  - Your results are more trustworthy, anybody can verify it!

- **It works**
  - We have actually more projects, and more funding due to open source activities
  - We were able to start many interesting and fruitful collaborations

- **It helps others as well**
  - Many companies, universities, individuals are using pieces of PULP, even commercially
PULP uses a permissive open source license

- All our development is on GitHub
  - HDL source code, testbenches, software development kit, virtual platform
    - https://github.com/pulp-platform
- PULP is released under the permissive Solderpad license
  - Allows anyone to use, change, and make products without restrictions.
PULP has released a large number of IPs

### RISC-V Cores
- RI5CY: 32b
- Ibex: 32b
- Snitch: 32b
- Ariane + Ara: 64b

### Platforms
- **Single Core**
  - PULPino
  - PULPissimo
- **Multi-core**
  - Fulmine
  - Mr. Wolf
- **Multi-cluster**
  - Hero
  - Open Piton

### Interconnect
- Logarithmic interconnect
- APB – Peripheral Bus
- AXI4 – Interconnect

### Peripherals
- JTAG
- SPI
- UART
- I2S
- DMA
- GPIO

### Accelerators
- HWCE (convolution)
- Neurostream (ML)
- HW Crypto (crypto)
- PULPO (1st ord. opt.)
How open source HW shaped our work

- I have chosen seven (out of 37) chips we had as part of PULP
  - Tried to pick from different times, different uses and different technologies

- Each chip has its own story
  - I will concentrate mainly on the open source aspects

- In addition to their technical results, each chip taught us
  - Collaboration models
  - What works what does not

- Most of what I talk is available as open source
  - We will briefly talk about what can and can not be open sourced as well
#1 - Pulpv1 (2013) – The first chip

- Our first complete PULP chip
  - 4x OpenRISC cores
  - STM 28FDSOI technology (RBB)
  - Explores body-biasing

- Collaboration with STM (France)
  - They needed a complete system demo (more than ring oscillators)
  - Demo for technology capabilities

- Meant for an IC tester
  - Almost no I/Os
First steps to open source, how to start?

- **At this time nothing was released**
  - We were 100% sure it would become open source
  - But we had no idea how
    - What can we open source, and what not
    - We work for ETH Zurich, we have to ask their permission
  - We also did not have much idea about licensing

- **We need support of industry**
  - This project was supported by ST Microelectronics
    - They would not support a project where they can not use our work ‘freely’
  - Permissive licenses are the only way
    - Even though purists consider it not ‘free’ enough
#2 – Fulmine (2015) – The award winning one

- **UMC65**
- **Technically similar to PULPv1**
  - 4x OpenRISC cores (still not RISC-V)
  - 2x HW accelerators
    - HW – Crypt (together with TU-Graz)
    - HW – Convolution Engine
- **Meant as a chip for boards**
  - Not only on a tester for characterization
  - Followed Mia Wallace, Honey Bunny
  - Paved the way for next wave of chips

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We have a base to work on and expand

- Much more than a core
  - Peripherals (SPI, UART, I2C, I2S)
  - DMA, Busses, event unit
- First chip with accelerators
  - Simple connection to the memory
  - Allows independent systems (HWCrypt/HWCE) to be added easily.
- Still not openly released
  - Using our OpenRISC core (3rd gen)
First open source release comes at this time

- **PULPino** was the first release (February 2016)
  - Used the SoC infrastructure and peripherals
  - Much simpler: single core, separate data, instruction memories

- **It is still the most popular release (name recognition wise)**
  - We have much more advanced releases, but PULPino is much better known
  - Your first release will end up carrying a lot of weight

- **Used SolderPad as a license**
  - Our friends at LowRISC suggested this license
  - Additions to Apache to clarify hardware related issues
  - We still use the same license
#3 - Mr. Wolf (2017) – The application chip

- TSMC40 LP
- One cluster with
  - 8 RISC-V cores
  - 2x shared FPU units
  - 64 kByte of TCDM
- One controller with
  - 512 kByte L2 RAM
  - Peripherals
- On chip voltage regulators
  - By Dolphin Integration

Mr. Wolf has been used in multiple systems

- Designed as an application processor
  - We still build boards with it
  - Despite only 200 manufactured

- Widespread industrial use:
  - Dolphin IP was validated on this chip
  - Greenwaves GAP8 is based on the open source release OpenPULP
  - BitCraze AI Deck is related
  - GAP9 (Vega) is a follow up project
What a difference two years make

- With Mr. Wolf, most of what we have is open sourced
  - This is a complex IoT processor, not like the much simpler PULPino
  - 8 + 1 cores, FPUs, shared accelerators, multiple power down modes.

- The cores are now RISC-V
  - Supports RV32IMCF and custom extensions (xPULP)

- Interesting collaboration with Dolphin Integration (SOITEC)
  - They have their IP demonstrated on a complex design, they can freely share
  - We get to use industrial IP in our chip

- Still many parts can still not be open source
  - FLL, analog macros, I/O cells, memory cuts (affects performance), P&R scripts
#4 - VivoSoC 3.142 (2019) – Analog and Digital

- Actually 4+ VivoSoCs since 2015
- SMIC 130/110 technology
  - Many Analog IPs
    - ExG interfaces, A/D converters
    - Pulse Oximetry
    - Neuro stimulators
- PULP cluster for post processing
  - 4x RISC-V cores
  - Digital interfaces
  - DMA transfer from analog block to digital

PULP allows us to co-operate with everyone

- Collaboration between Prof. Benini and Prof. Huang
  - Permissive licensing allows collaboration even if the result is not open source
#5 - Arnold (2018) – Fastest collaboration

- **GF22nm**
  - RISC-V microcontroller with eFPGA
  - Based around PULPissimo

- **Collaboration with Quicklogic**
  - Met at GTC 2017 by coincidence
  - In one year chip was taped out
  - Only possible because of open source nature

- **Quicklogic is going open source**
  - They announced June 2020 the Quicklogic Open Reconfigurable Computing
  
  [https://www.quicklogic.com/QORC/](https://www.quicklogic.com/QORC/)
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PULPissimo: very good platform for extensions

- eFPGA added as accel.
  - Easy plug and play
  - Configuration over APB
  - Additional ALU and memory
  - Uses the same memory

- Multiple operation modes
  - Configurable peripheral
  - Accelerator for core
  - Accelerator for independent I/O
#6 - Rosetta (2019) – The academic collaboration

- TSMC65 chip using PULPissimo
- Contains independent blocks
  - ESL from EPFL
  - TCL from EPFL
  - Two separate projects from us
  - All sharing the same infrastructure
- Each attached independently
  - Individual projects are not related
  - They all make use of processor, memory, debug infrastructure

Publication in preparation
Open source collaboration scheme explained

Direct research collaborators on PULP

- Politecnico di Torino
- University of Cambridge
- EPFL Lausanne
- CSEM Neuchatel
- TU Kaiserslautern
- University of Cagliari
- IBM Research Zurich
- CEA-Loi Grenoble
- Fraunhofer-Gesellschaft
- Sapienza Università di Roma
- Princeton University
- Technische Universität Graz
- Politecnico di Milano
- Fondazione Bruno Karsner
- Lund University

Academic users we are aware of

- Università di Genova
- Stanford University
- UC Los Angeles
- UC San Diego
- Columbia University
- Universitat Bar-Ilan
- Istanbul Teknik Universitesi
- NCTU Hsinchu
- University of Zagreb, FER
- TUT Tampere
- TU Darmstadt
- RWTH Aachen
- Universität Bremen
- IST University of Lisboa
- Hengik University Seoul
- UFRN Rio Grande do Norte
- ITI Kharagpur
- LIRMM Montpellier
- University of Stuttgart
- University of Tübingen
- FORTH Hellas
- Chalmers Göteborg
- Kyoto University
- FAU Erlangen-Nürnberg
- NTNU Trondheim

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Open source collaboration scheme explained

Industrial users of PULP

- OPENHW
- lowRISC
- Google
- Mentor
- cadence
- QuickLogic
- IBM
- NXP
- GREENWAVES TECHNOLOGIES
- onespin
- imperas
- SILICON LABS
- STMicroelectronics
- GLOBALFOUNDRIES
- EMBECOSM
- axiomise
- ASHLING
- ACP AG
- DOLPHIN INTEGRATION
- CEVA
- Valtrix
- antmicro
- WITTENSTEIN

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#7 - Baikonur (2019) – Globalfoundries and ETH

- 2x 64bit Ariane cores
- GF uses to validate flow
  - One core optimized for high performance (HP)
  - One core for low power (LP)
- ABB IP by INVECAS
  - Automated Body Biasing
  - Various test modes to characterize
- Additional payload
  - 3x clusters of 8x Snitch clusters
  - 1.25 Mbyte memory shared for all

Ariane is one of our most popular cores

- Linux capable RV64GC core
- FPGA port
  - Xilinx Genesys
- Used in many projects:
  - EPI
  - Hensoldt Cyber (Mig-V)
  - OpenPiton (Princeton)
Graduating our cores for a better future

- Several of our open source cores are maintained by others
  - Zero-riscy became Ibex and is maintained by LowRISC
  - RI5CY became CV32E40P and is maintained by OpenHW group
  - Ariane (recently) became CVA6 and is maintained by OpenHW group

- This is an excellent opportunity for us
  - These groups have funds to support much needed but tedious work
    - Documentation, verification, user support

- Also means that we have done a good job 😊

- And creates opportunities for our graduates
  - At the moment Pirmin, Davide S., Florian are involved
LowRISC and OpenHW are essential for us

Example
Although Zero-Riscy was open source since 2016, work on it really picked up when LowRISC took over.

35+ Contributors
1300+ Contributions
470 GitHub Issues

This amount of work does not come from volunteer efforts for all projects.
Open HW Group

- **OpenHW Group** is a not-for-profit, global organization (EU, NA, Asia) driven by its members and individual contributors where HW and SW designers collaborate in the development of open-source cores, related IP, tools and SW such as the Core-V family of cores.

- **OpenHW Group** provides an infrastructure for hosting high-quality open-source HW developments in line with industry best practices.

- Many partners

- Many more resources

- Also to the work that we normally don’t done

- Verification, documentation

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Multi-B$ companies using (or planning) our cores in their products!

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We benefit from our open source activities

- **Science**
  - Community building, sharing ideas
  - Reduce "getting up to speed" overhead
  - Work on things that make a difference
  - Fair benchmarking

- **Society**
  - More innovation, growth, jobs
  - Bridges the gap between groups, allows more people to contribute
  - More secure, safe auditable HW

- **Business**
  - Reduce NRE costs for silicon
  - Faster innovation paths for startups
  - New business models
  - Helps exchange ideas across NDA walls
Luca Benini, Davide Rossi, Andrea Borghesi, Michele Magno, Simone Benatti, Francesco Conti, Francesco Beneventi, Daniele Palossi, Giuseppe Tagliavini, Antonio Pullini, Germain Haugou, Manuele Rusci, Florian Glaser, Fabio Montagna, Bjoern Forsberg, Pasquale Davide Schiavone, Alfio Di Mauro, Victor Javier Kartsch Morinigo, Tommaso Polonelli, Fabian Schuiki, Stefan Mach, Andreas Kurth, Florian Zaruba, Manuel Eggimann, Philipp Mayer, Marco Guermandi, Xiaying Wang, Michael Hersche, Robert Balas, Antonio Mastrandrea, Matheus Cavalcante, Angelo Garofalo, Alessio Burrello, Gianna Paulin, Georg Rutishauser, Andrea Cossettini, Luca Bertaccini, Maxim Mattheeuws, Samuel Riedel, Sergei Vostrikov, Vlad Niculescu, Hanna Mueller, Matteo Perotti, Nils Wistoff, Luca Bertaccini, Thorir Ingulfsson, Thomas Benz, Paul Scheffler, Alessio Burello, Moritz Scherer, Matteo Spallanzani, Andrea Bartolini, Frank K. Gurkaynak, and many more that we forgot to mention

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