Building the Road from Computer Architecture to Silicon at BSC

Workshop on RISC-V and OpenPOWER
ICS 2020, 29 June 2020, Barcelona

DRAC project – Designing RISC-V-based Accelerators for next generation Computers

Miquel Moretó
Francesc Moll

Barcelona Supercomputing Center
Centro Nacional de Supercomputación

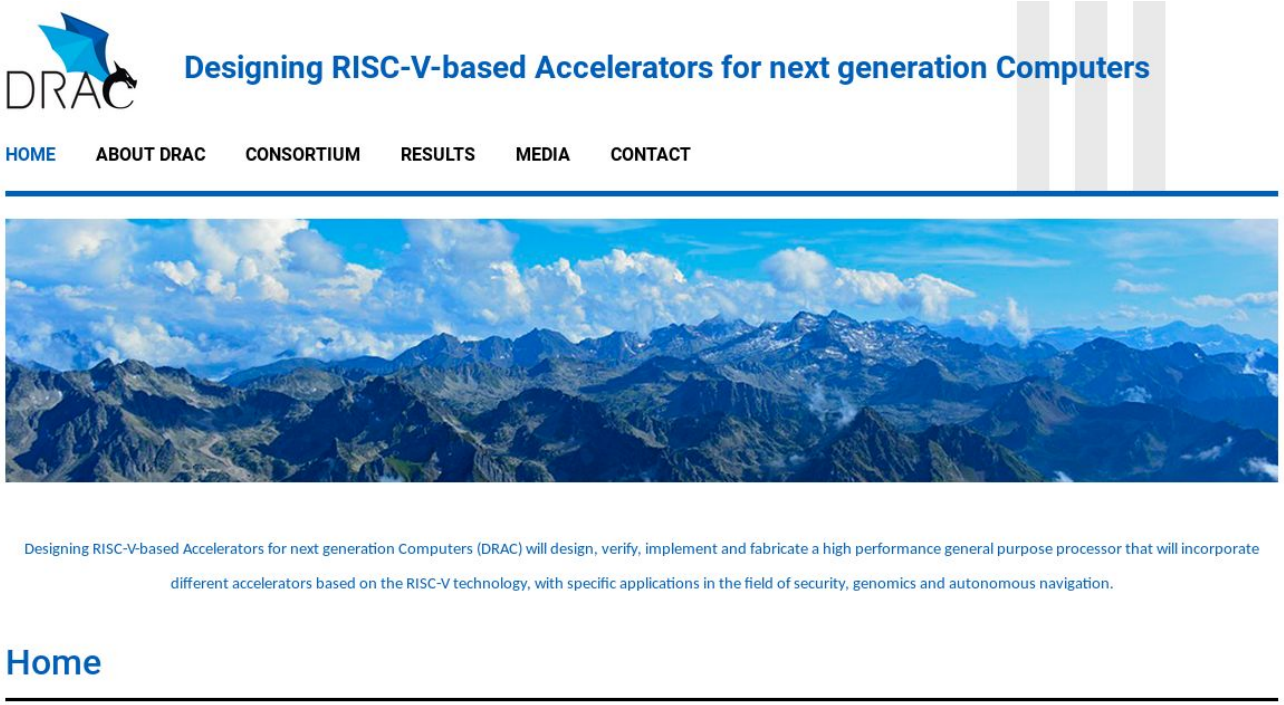
UNIVERSITAT POLITÈCNICA DE CATALUNYA
BARCELONATECH

Outline

- DRAC goals
- Architecture to (custom) silicon
- First silicon at BSC: preDRAC RISC-V processor
- Next Tapeout
- Future steps

DRAC project (2020-2023)

- Catalan consortium, co-funded (50%) by ERDF funds from Generalitat de Catalunya
- Bring to silicon a RISC-V OoO processor and a number of accelerators:
  - Post-Quantum cryptography
  - Genomics
  - Autonomous navigation



https://drac.bsc.es

Barcelona Supercomputing Center
Centro Nacional de Supercomputación

UAB Universitat Autònoma de Barcelona

Universitat de Barcelona

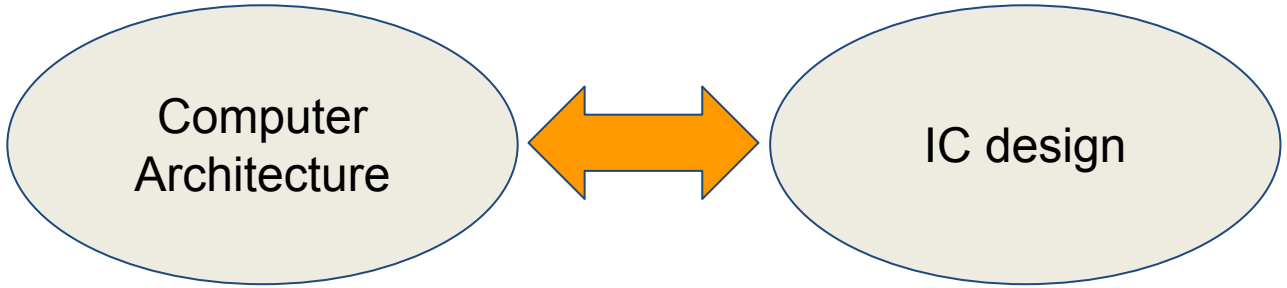
Universitat Politècnica de Catalunya BarcelonaTech

Universitat Rovira i Virgili

DRAC

Why build an IC design team at BSC?

- Timing, power and area are very much technology-dependent
- Link between architecture and physical effects
- Provide early feedback on architectural choices

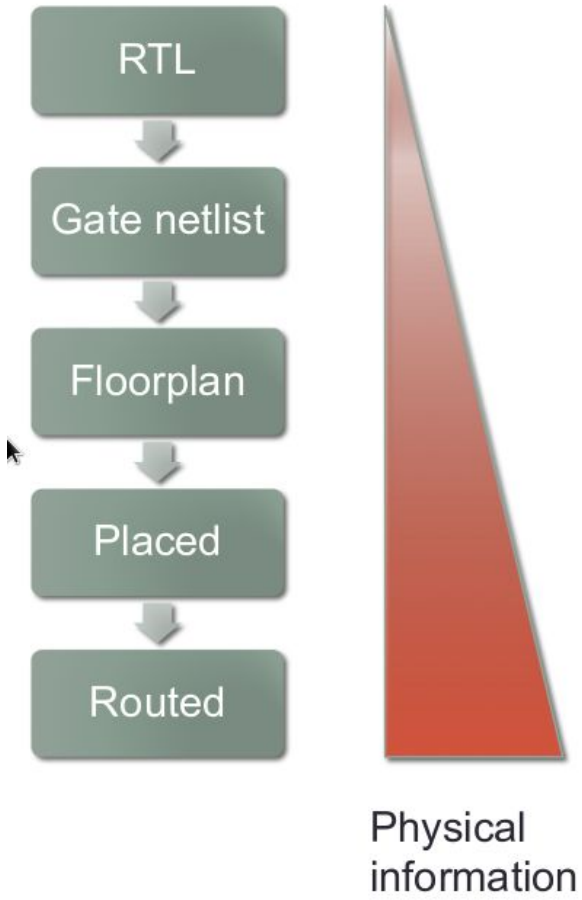


- Work on actual systems with concrete application and specs
- Test new ideas on actual systems, in silicon
- Training future researchers in design methods.

Overall goal: generate better processors matching architecture proposals to technological capabilities, in line with leading research institutions.

Needed expertise for IC design

- FPGA for fast prototyping
- Technology-dependent libraries
  - Timing & Power (lib)
  - Physical (lef)
  - Physical IP (macros)
  - Corners
- Technological issues
  - Testability
  - Manufacturability
  - Signal integrity
  - Low power
  - Custom analog IP

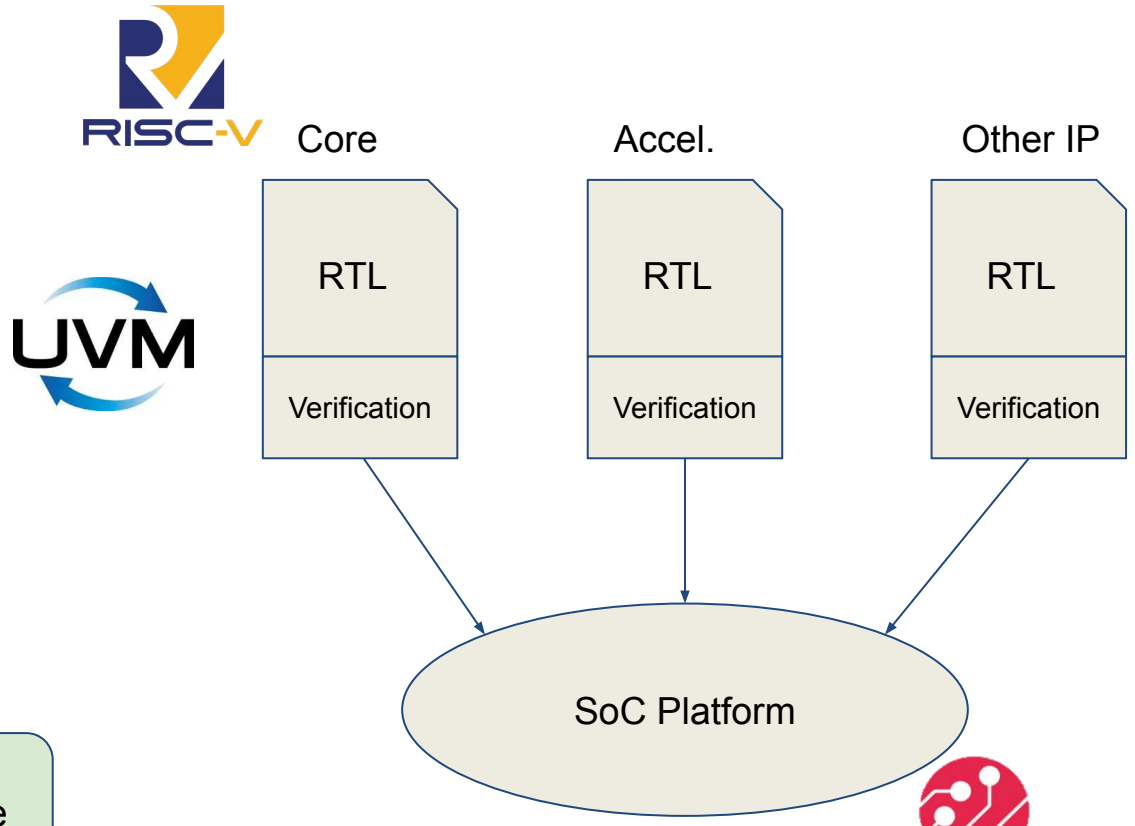


Components to design a SoC processor

- Core processor
- Interconnect bus
- Interfaces
  - Main memory (DRAM)
  - Host computer
  - Other peripherals
- Accelerators

- SoC platform

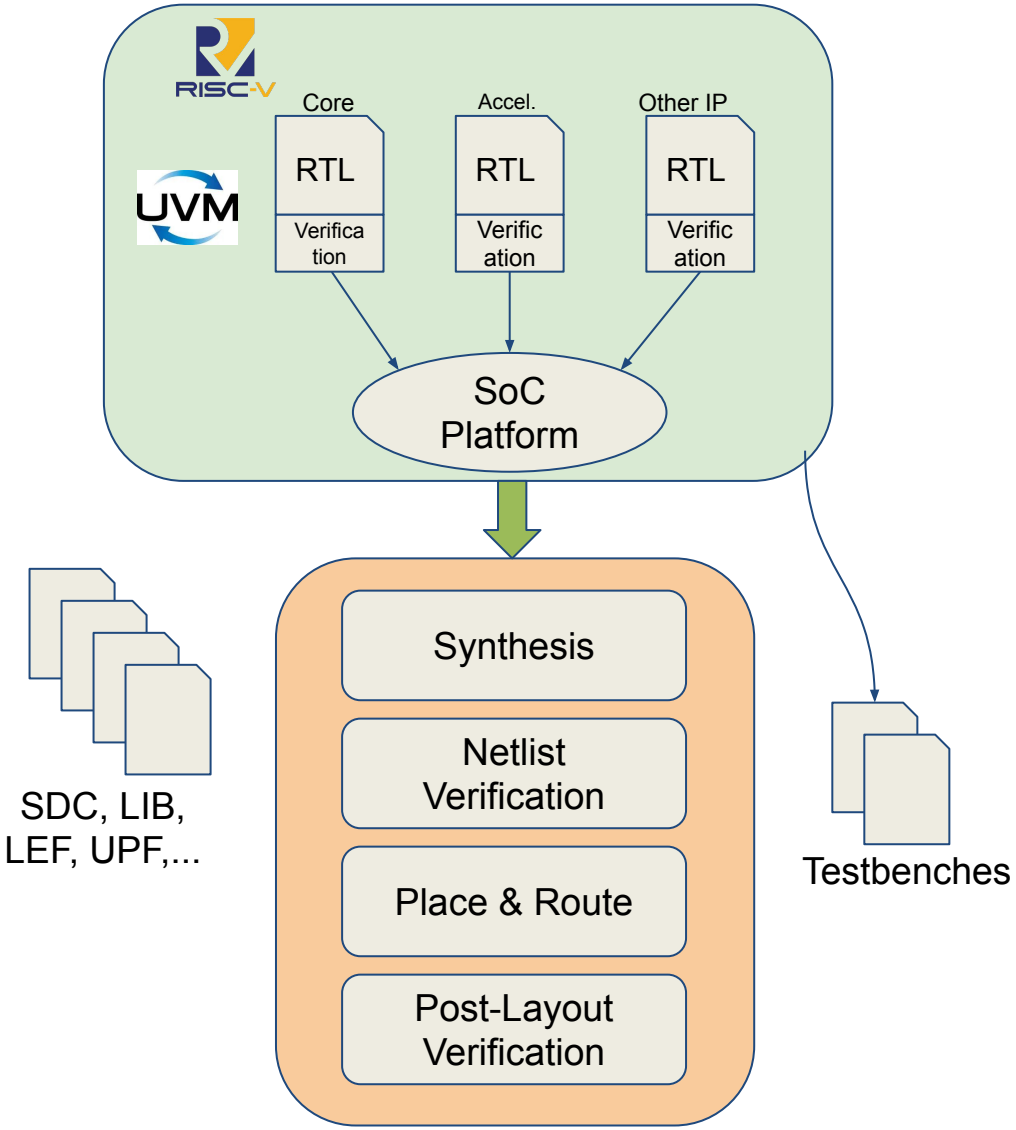
Many Open-Source options



Components for physical design

- Technology libraries
- Physical macros
  - SRAM...
- Analog IP
  - PLL, sensors...
- Constraints
- Test specifications
- Low Power specifications

Mostly proprietary IP



First BSC tapeout: building the IC design team

- Leverage IC design expertise in local partners
  - UPC
  - IMB-CNM
- Access to design tools and manufacturing through Europractice
  - Tech libraries
  - MPW manufacturing

- CAD engineering
- Synthesis
- Place & Route
- Netlist Post-Layout verification

~ 5-8 people

Design, platform integration, Verification

~ 30 people

PreDRAC chip partners

Main objective: design, verify and fabricate a first RISC-V academic processor in Spain

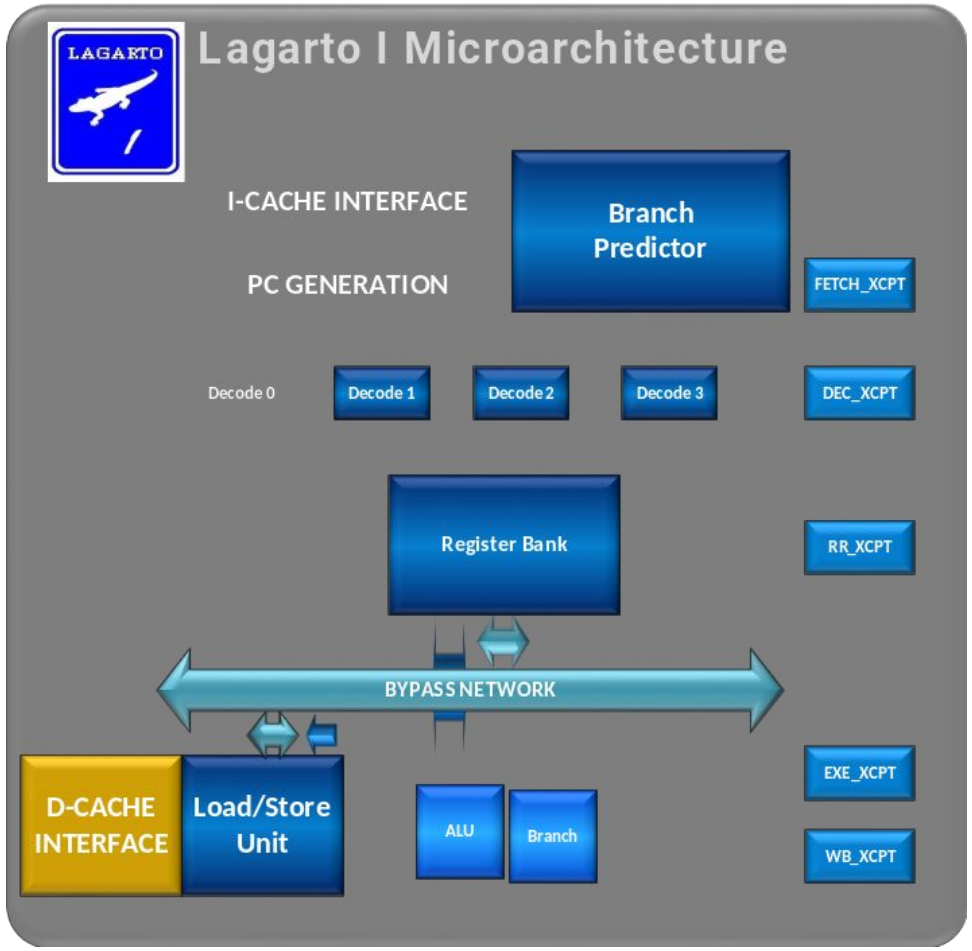
Partnership with:

Barcelona Supercomputing Center (**BSC**)
Universitat Politècnica de Catalunya (**UPC**)
Centro Nacional de Microelectrónica (**IMB-CNM**)
Instituto Politécnico Nacional de México (**CIC-IPN**)

~40 people involved

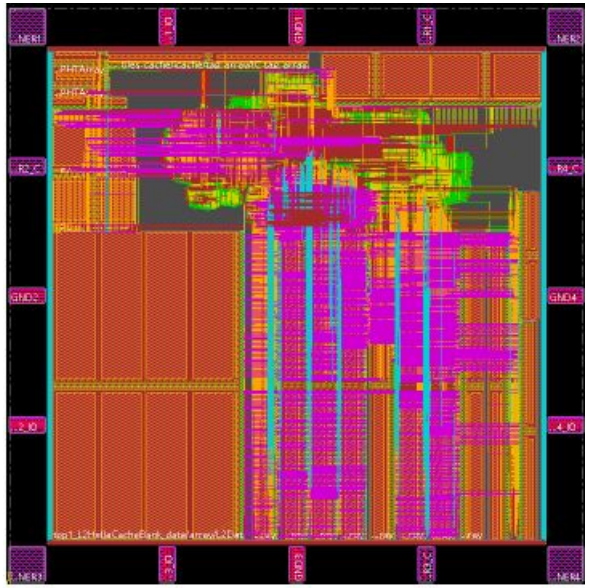
PreDRAC core: Lagarto I

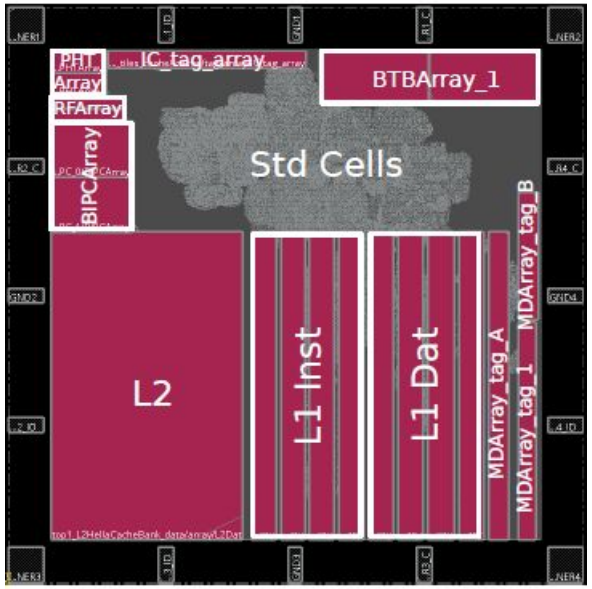
- **Lagarto** Core
- RV64IMA **RISC-V**
- 5 stage **in-order** pipeline
- Written in **Verilog**



First tapeout: preDRAC SoC

- Target technology: TSMC 65nm
  - Design fits in the total area budget of 2.5 mm^2 (core), 4 mm^2 (total)
  - Tapeout: May 15 2019
  - Returned: Early September 2019
- Collaborative project with different teams:
  - RTL Design: Lagarto (BSC + CIC-IPN)
  - Verification (BSC)
  - Logic Synthesis (UPC + BSC)
  - Physical design (IMB-CNM + BSC)
  - Tapeout and bringup (IMB-CNM + BSC)

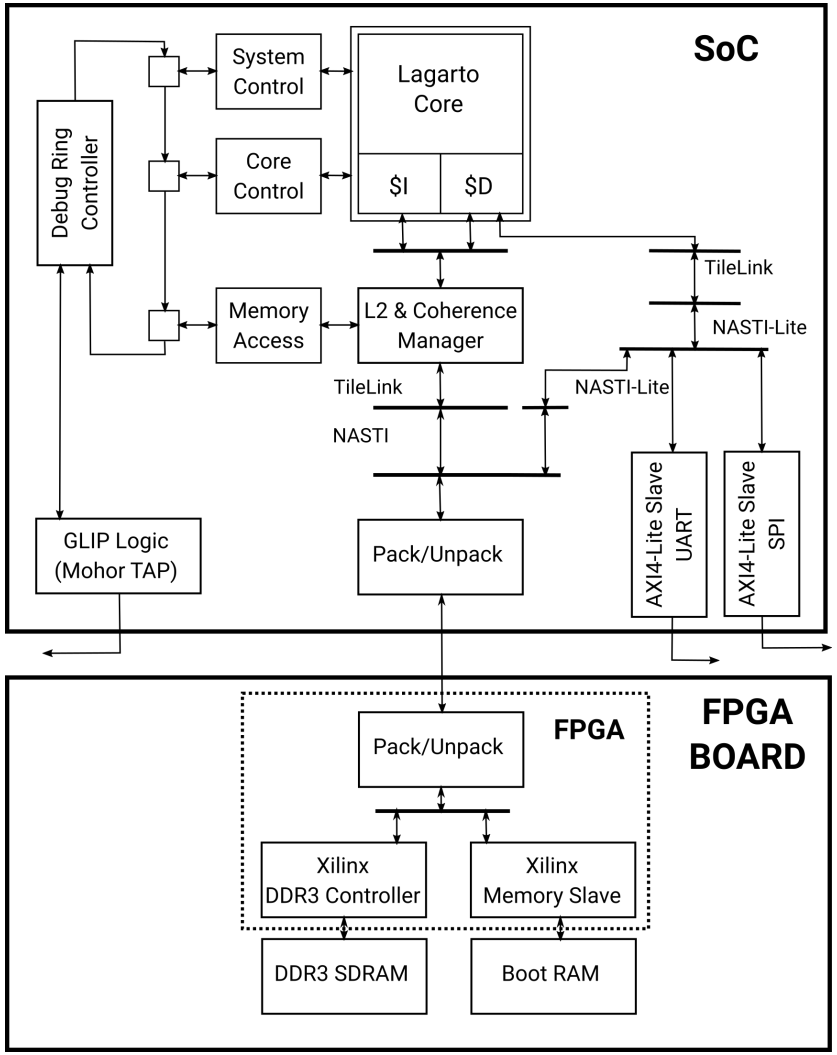




First tapeout: preDRAC SoC

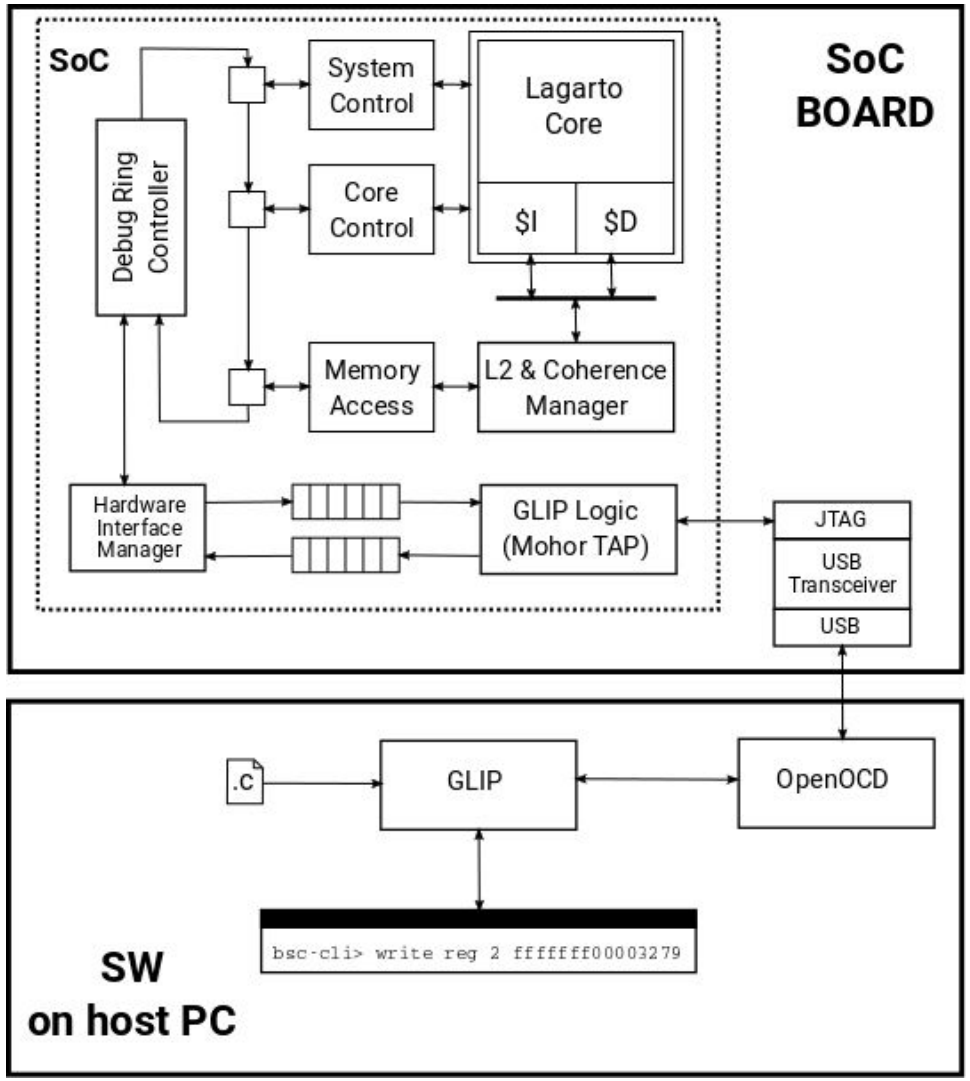
- Linux-capable System-on-Chip based on lowRISC 0.2

  - Lagarto In-order core
  - 16 kB L1 Dcache/Icache
  - 64-kB L2 Unified Cache
  - Custom SPI & UART controllers
  - JTAG & Debug ring
  - Performance monitoring counters



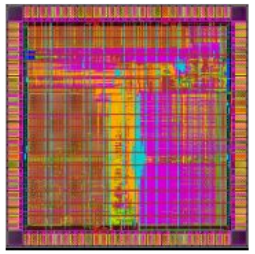
SoC Debug ring

- RTL internally developed since lowRISC DR was only available as bitstream
- Needed for Linux booting operations

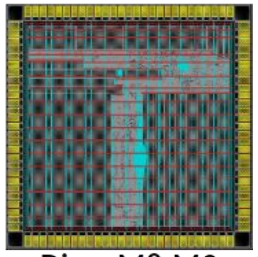


preDRAC SoC Layout

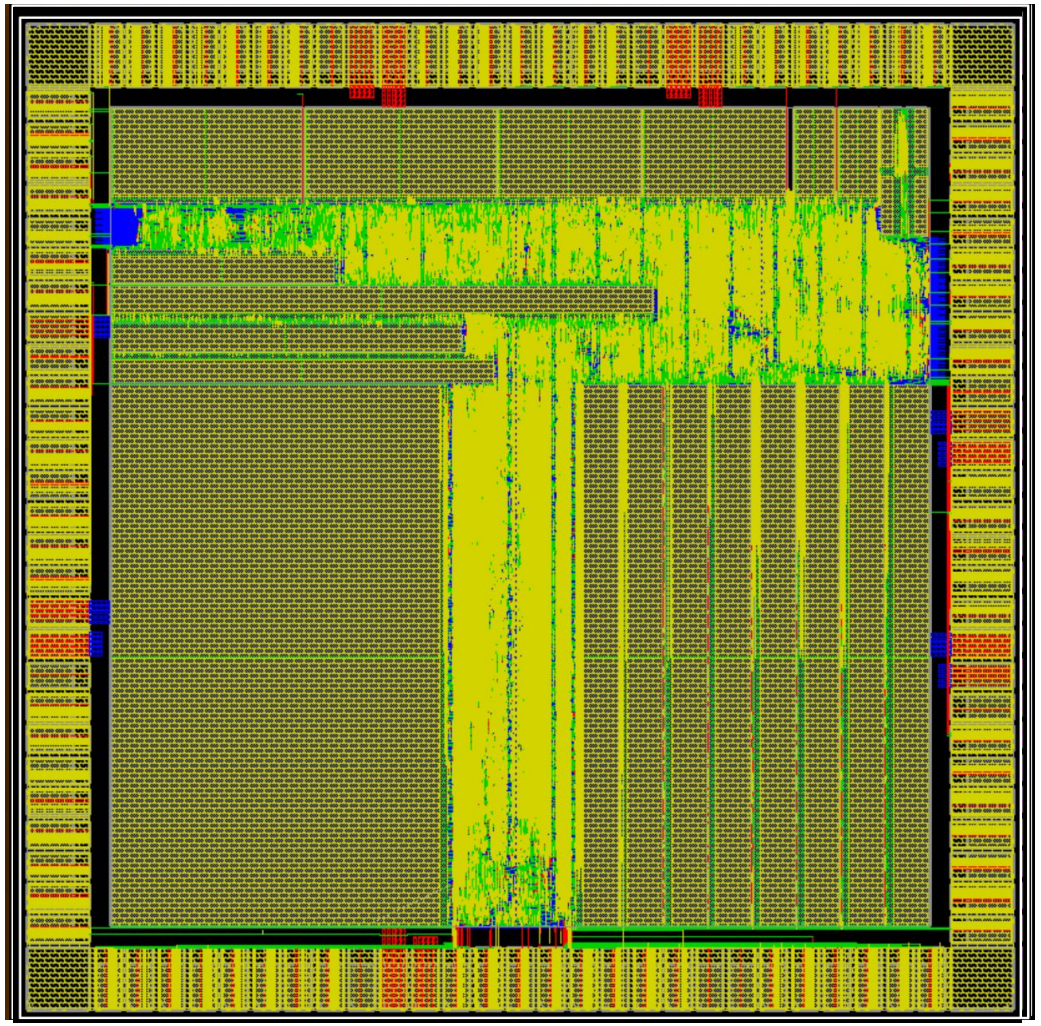
Die - TOP

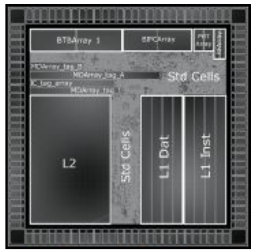


Die - All

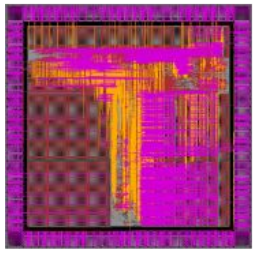


Die – M8-M9

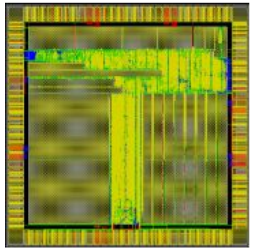




Die - Floorplan



Die – M5-M7



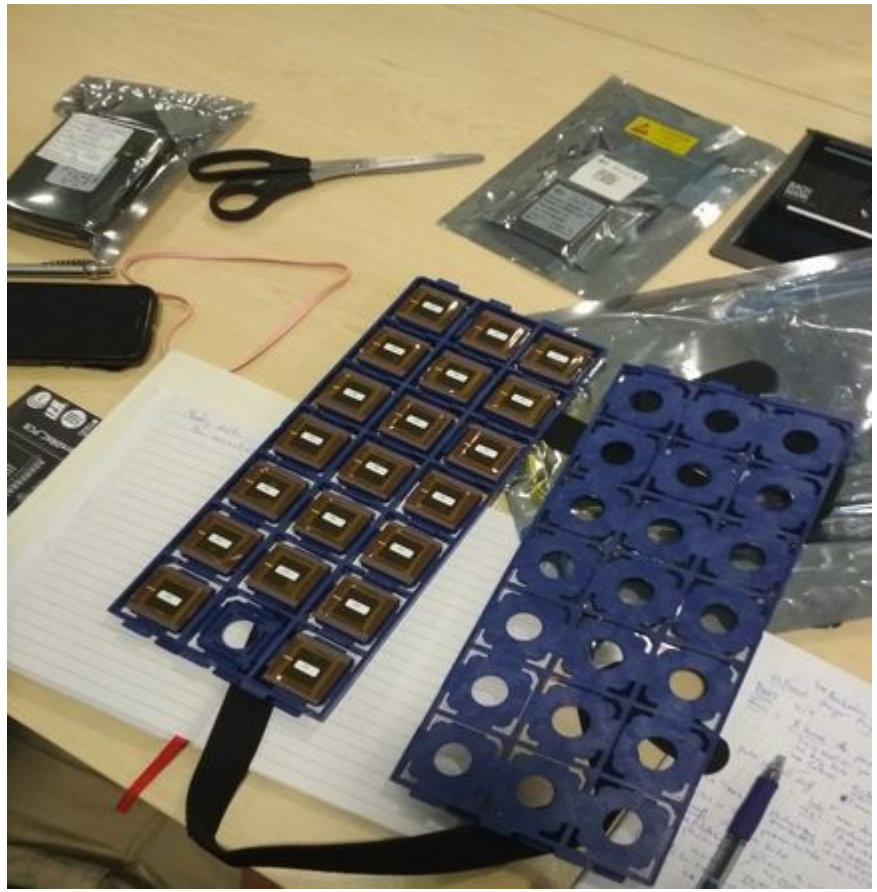
Die – M1-M4

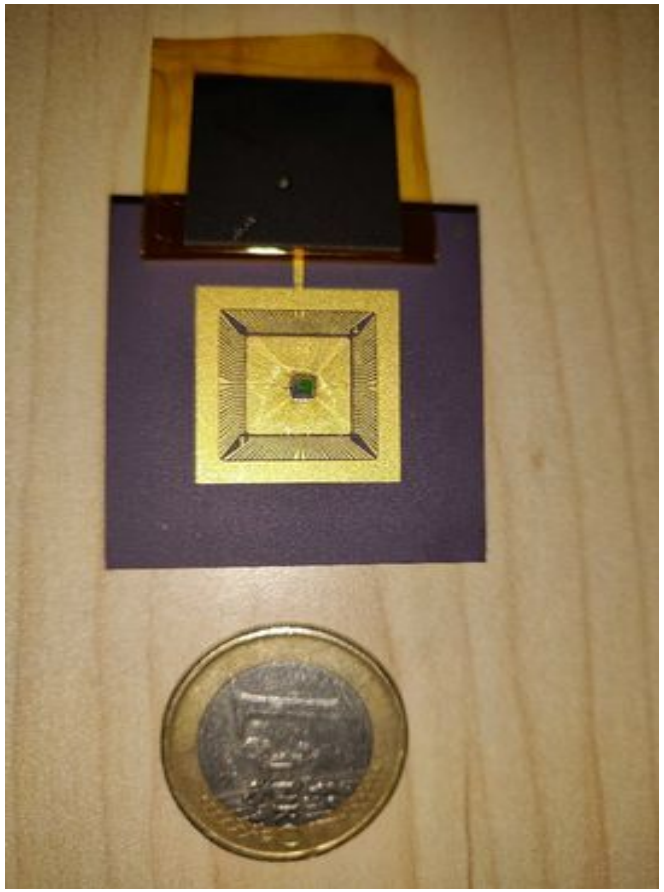
preDRAC manufacturing

- Europractice mini@sic MPW
  - **TSMC 65nm**
  - 2mm x 2mm
  - Target **200MHz**
  - CPGA120 package
  - **Submission 15th of May 2019**

Images courtesy of CNM

preDRAC packaging





preDRAC SoC die

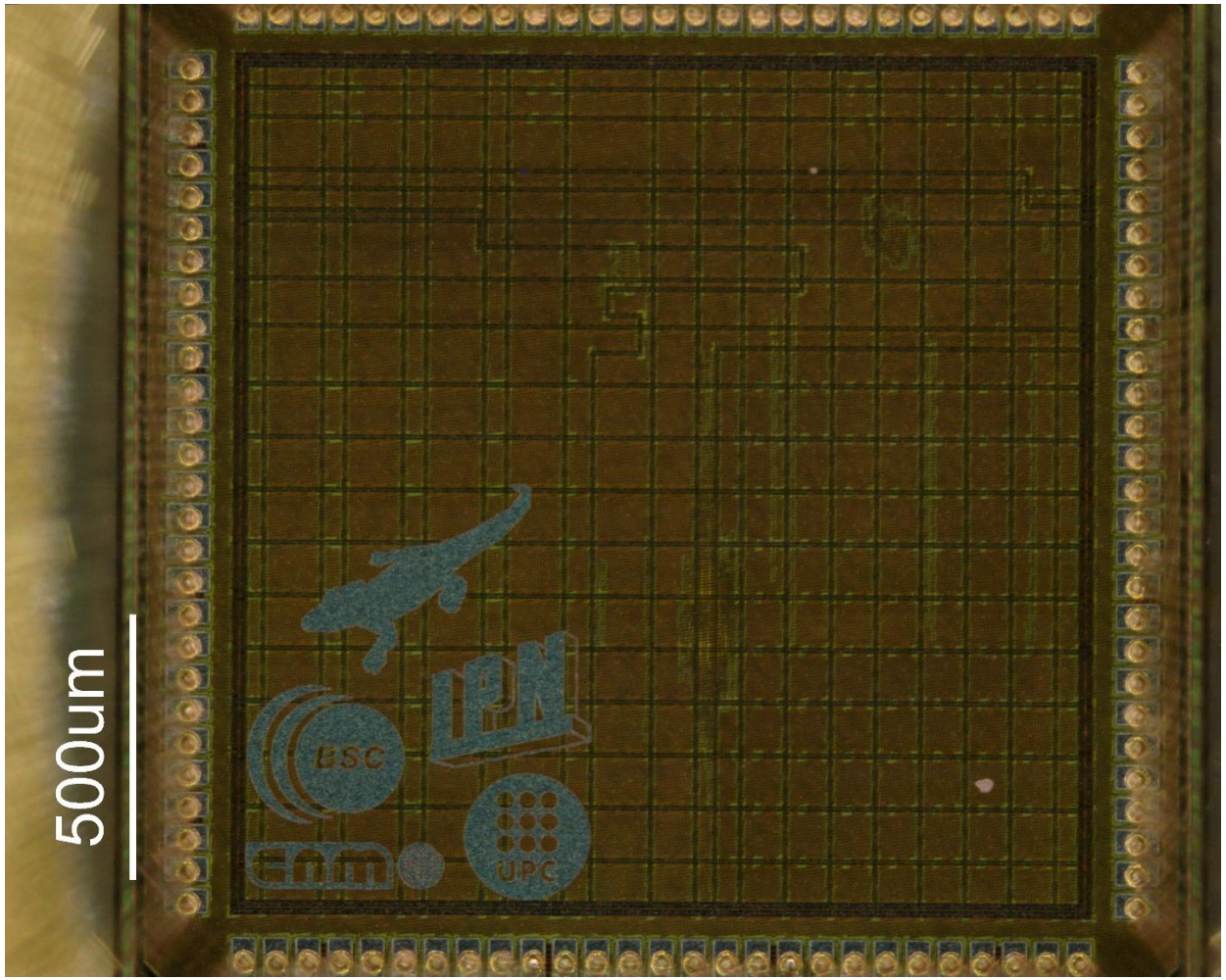
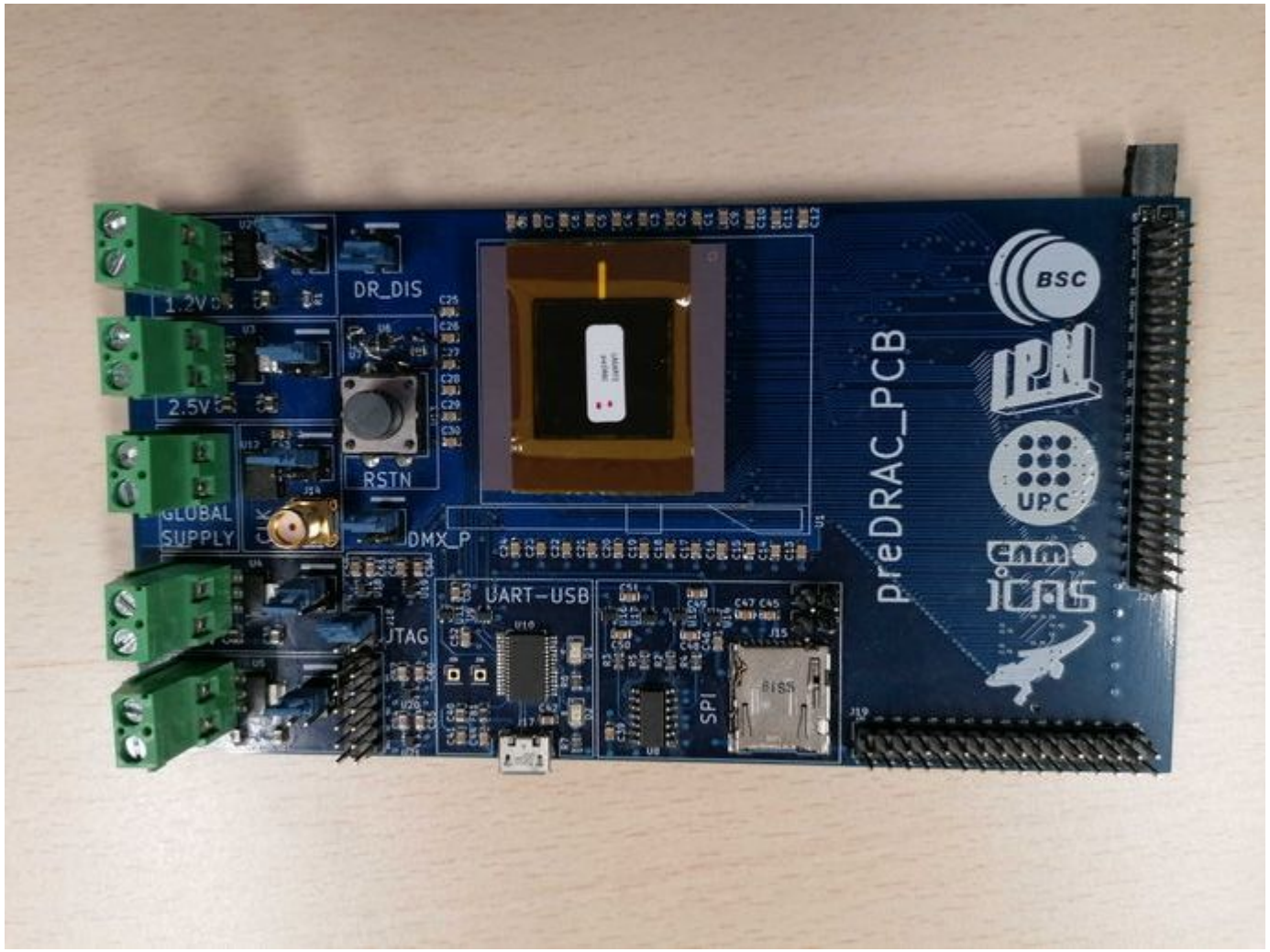
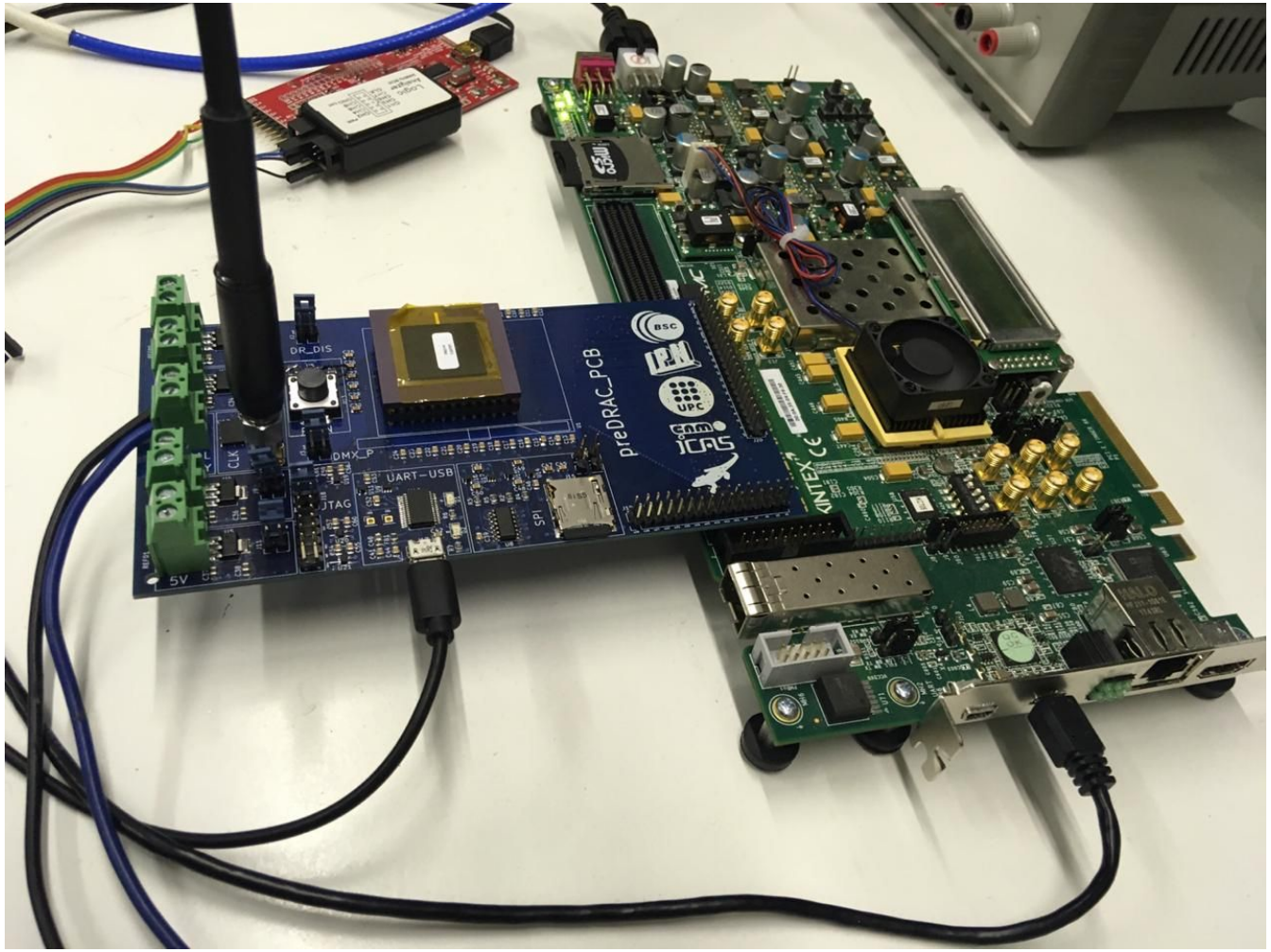


Image courtesy of CNM

Bringup board



FPGA board host for main memory

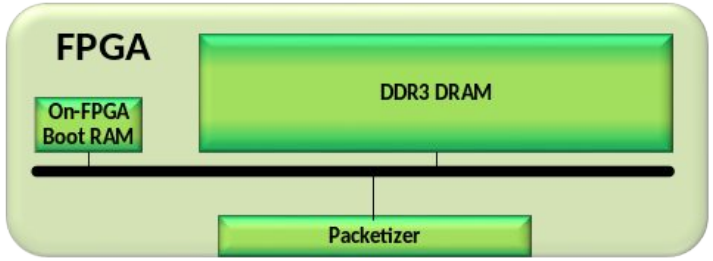


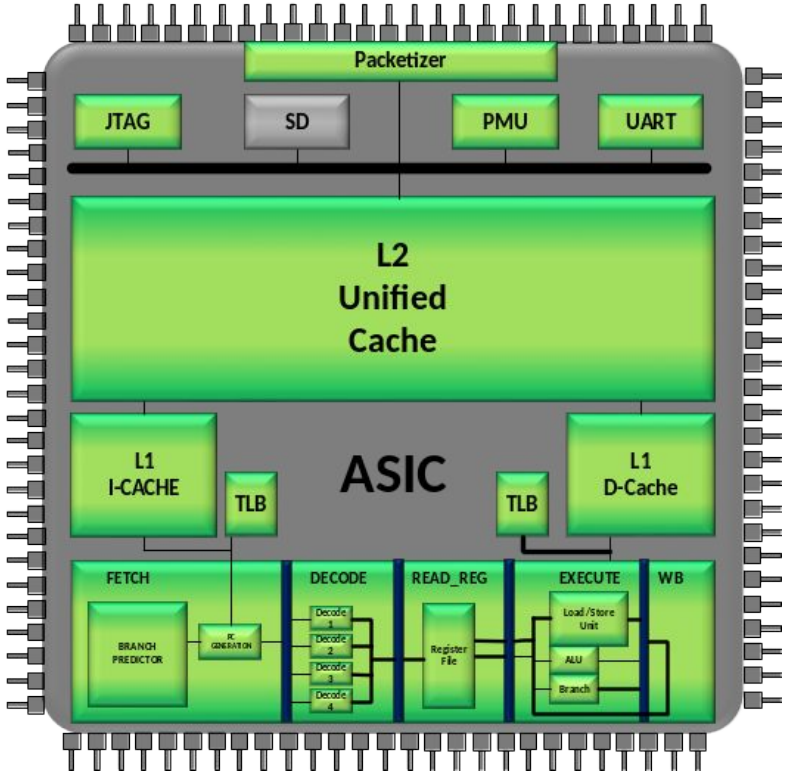
Functional test

- What is working?
  - Lagarto pipeline
  - L1 Icache/DCache
  - L2 Unified Cache
  - JTAG & Debug-ring
  - UART
  - PMU
  - Packetizer

Bare-metal applications:

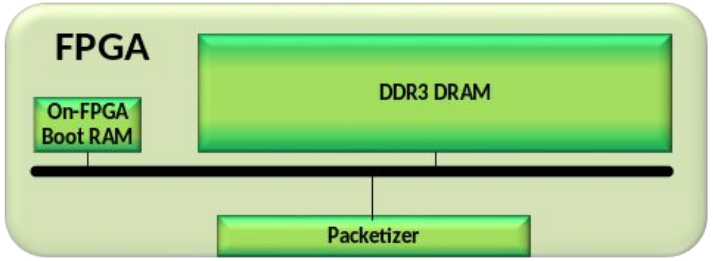
  - Matrix Multiplication
  - Bubble sort
  - Tower of Hanoi

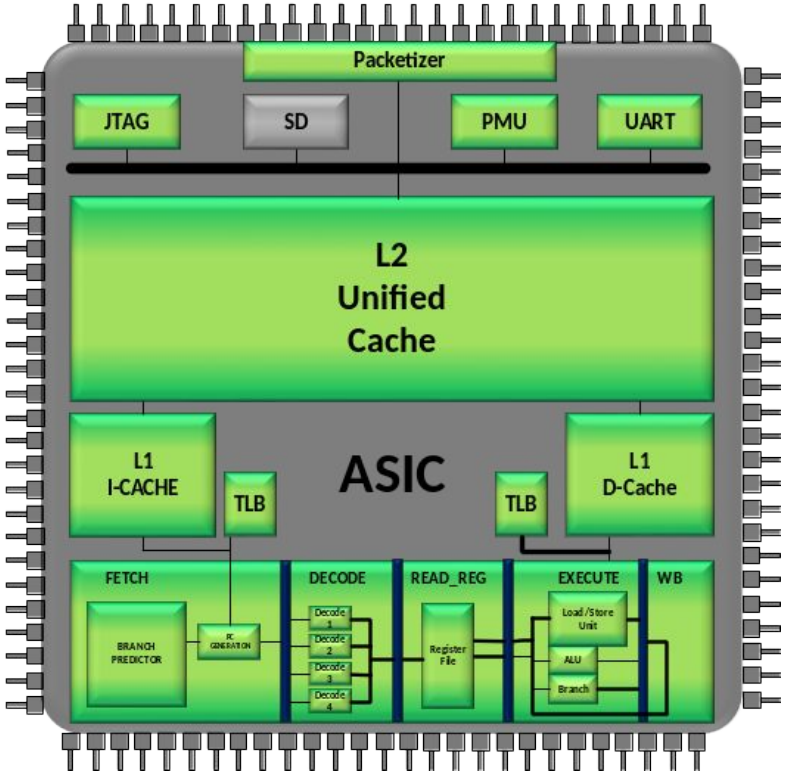




Linux boot

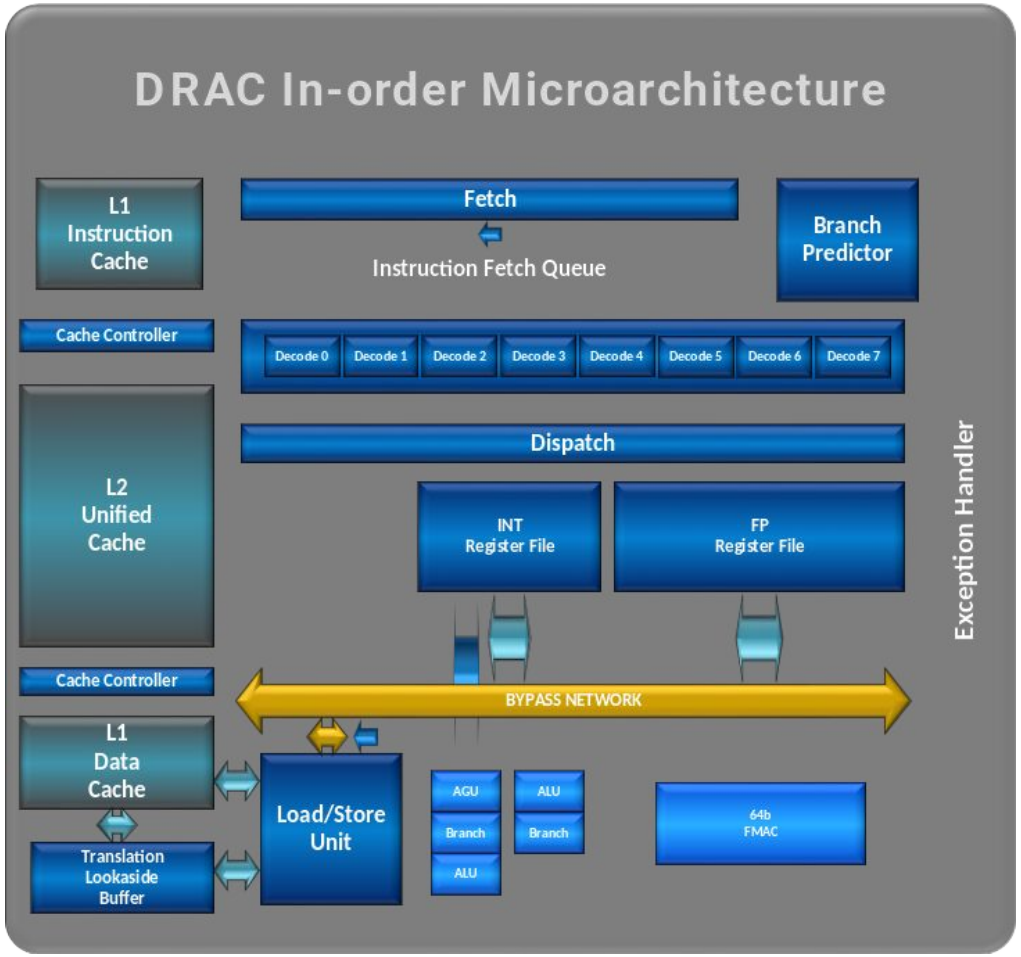
- Original plan was to use the on-chip SD card (SPI) interface (not working)
- Workaround: use the FPGA board SD card, accessing it via the Packetizer
  - UART and SPI controller implemented in FPGA
- Linux successfully boots using BusyBox version 1.21.1, Linux kernel version 3.14.41, and a riscv64-linux-gnu-gcc version 5.2.0.
- BusyBox allows to integrate custom "applets" that include the Matrix multiplication and the Coremark benchmarks.
- The Matrix multiplication yielded 0.32 IPC and the Coremark obtained 172 iterations per second execution time.





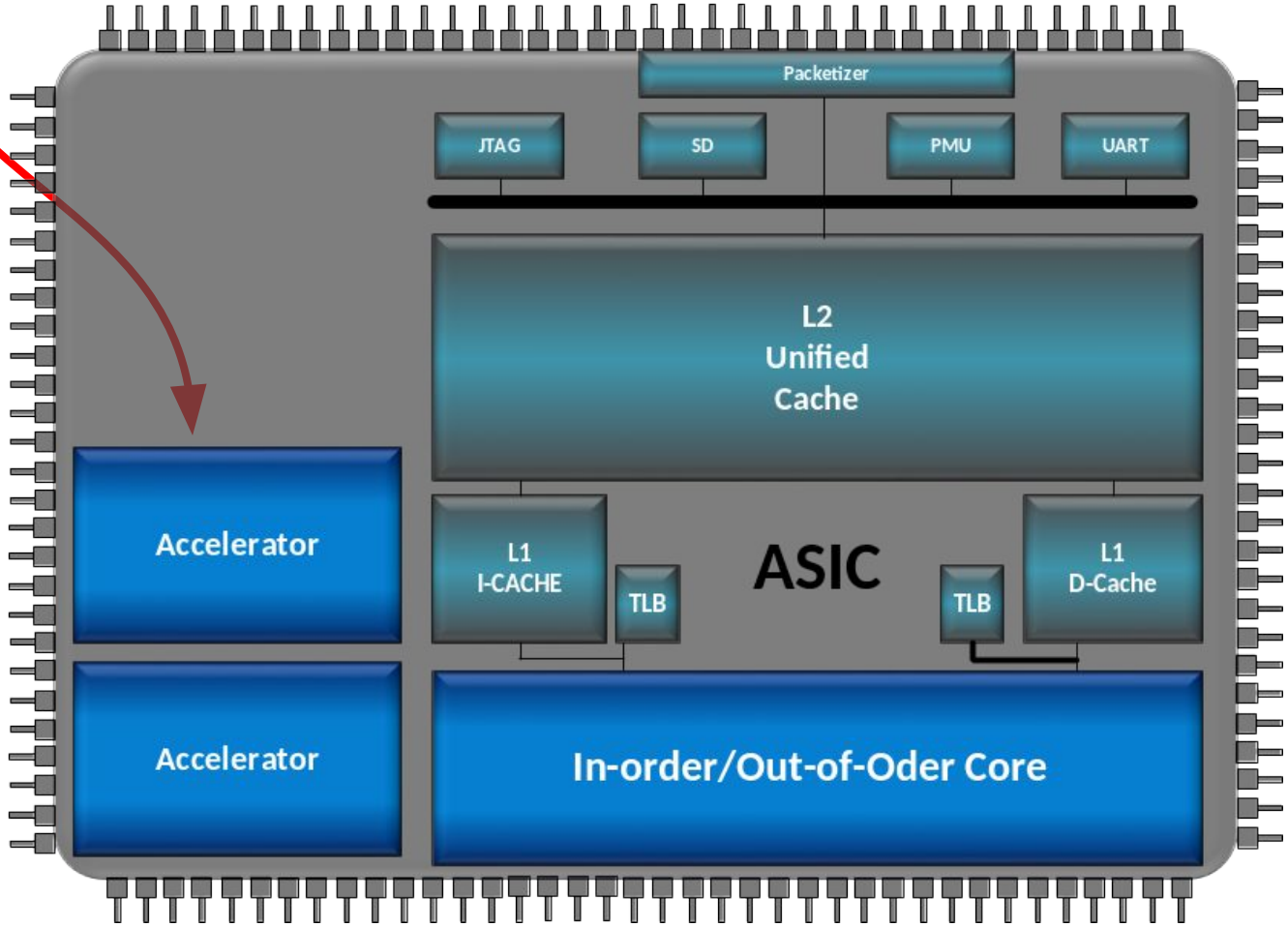
Next tapeout in TSMC 65nm

- Improved Lagarto in-order core, Power & Area optimized
- Newly developed IP:
  - SDRAM memory controller (BSC)
  - HyperRAM memory controller (BSC)
  - VGA (BSC)
  - PLL (CNM)
  - ADC (CNM)



Towards DRAC tapeouts: 22nm FDSOI

- **<u>Accelerators</u>** along the core



Silicon capabilities to be added during DRAC

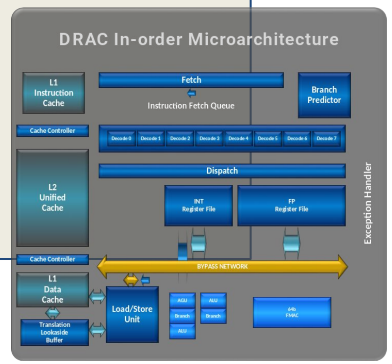
Target technology: GF 22nm FDSOI (22FDX)

- Design for Testability
- SerDes for high-speed interface to main memory
- Body Bias generator
- PV monitor
- PLL/clock generator
- On-chip sensors (T)
- ....

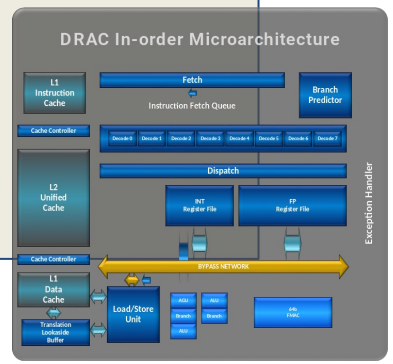
DRAC tapeouts roadmap

2020 2021 2022 2023

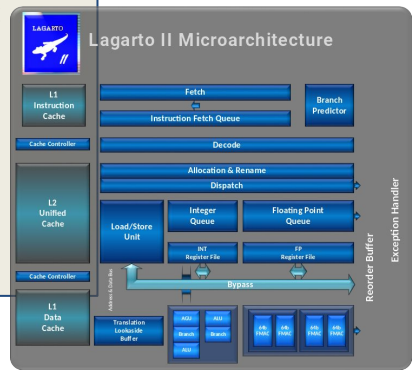
TSMC 65nm
- DRAC In-order
- PLL 600 MHz
- SDRAM mem cont
- HyperRAM
- ADC



GF 22nm FDSOI
- DRAC In-order
- PLL 1 GHz
- SDRAM/HyperRAM
- VPU
- SerDes 8 GHz



GF 22nm FDSOI
- DRAC out-of-order
- PLL 1 GHz
- Crypto Acc
- Genomic Acc
- Automotive Acc
- SerDes 8 GHz
- Body Bias



DRAC

PreDRAC design team (September 2019)

DRAC

Acknowledgment

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Departament d'Economia i Coneixement
Secretaria d'Universitats i Recerca

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