Barcelona Supercomputing Center
Centro Nacional de Supercomputación

EXCELENCIA SEVERO OCHOA

Workshop on HPC & RISC-V and OpenPOWER

John D. Davis, BSC

ICS International Conference on Supercomputing 2020

June 29 - July 2, 2020. Worldwide online event

Barcelona, 2020/06/29

But Wait, There's More

Surprise Announcement just for you!!!

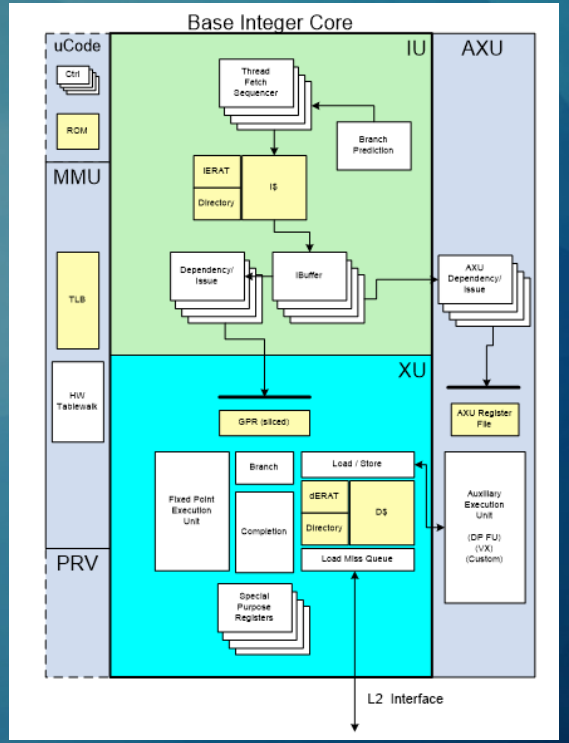
(new OpenPOWER core!)

A2I POWER Processor Core – Now Open!!

- Design optimized for high aggregate throughput
- Balanced performance and power with modular design
- Implemented in 45nm SOI (Silicon on Insulator)
- Developed for PowerEN (Edge-of-Network) “wire-speed processor” design
- Used in BlueGene/Q (HPC) as the general purpose processor

A2I Design Features

- 64-bit PowerISA v2.06 Book III-E
- 4W SMT, 2W issue
- In-order dispatch/execution w/dynamic branch prediction (8K BHT)
- L1: 16K 4W IC, 16K 8W DC, 64B line
- Modular design w/optional units for application-specific implementations
  - MMU: 512 x 4 TLB, 4TB physical addressability
  - AXU: tightly-coupled coprocessor interface, 32B L/S
  - Microcode engine
- Full support for both big and little endian byte ordering



45nm
Area = 2.9mm^2
3.0 GHz max
2.3 GHz @ .9W

7nm Estimation
Area = 0.17mm^2
4.2 GHz @ .5W
3.0 GHz @ .15W

Available Now OpenPOWER™

RTL, documentation, and FPGA environment (A2I core with AXI interface)

https://github.com/openpower-cores/a2i

Thank you!!

- 15 Academic and Industrial talks of Open Source ISAs and HPC
  - History, HW and SW building blocks, including CI/CD
  - Accelerators to CPUs
  - Ecosystem updates from OpenPOWER and RISC-V
- Talk slides and videos will be posted in the next few days
- Several announcements

Another Announcement

- RISC-V Special Interest Group on HPC
  - https://lists.riscv.org/g/sig-hpc
  - https://lists.riscv.org/g/sig-hpc/files/ (initial files: Mission, Charter, Roles)

- **Mission:** Provide a global forum for technical and strategic high performance computing, systems and components (processors, accelerators, etc.) targeting large scale performance (tera-, peta-, exascale, and beyond) and power targets (any data and compute intensive domains), imperatives to leverage and enable RISC-V.
  - Technical imperatives
  - Business imperatives

Some SIG-HPC RISC-V Technology Topics

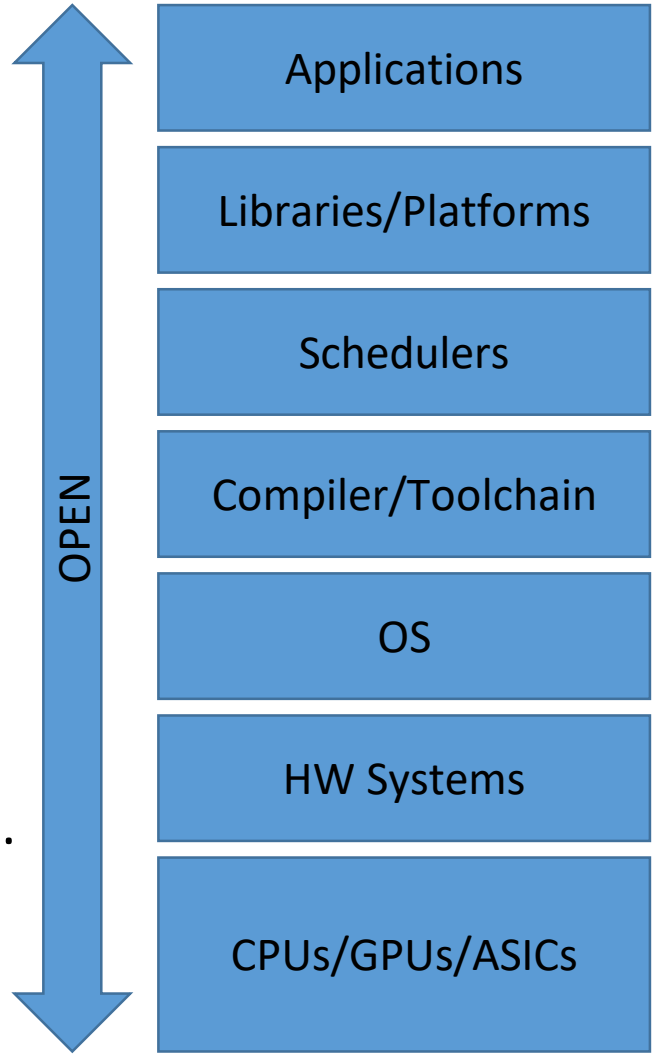
- Compute intensive applications and application domains HPC, including HPDA (AI/ML/DL).
- System software stack from applications, middleware and frameworks, to toolchains (compilers, debuggers, etc.), and board support packages (BSPs).
- Software ecosystem alignment and roadmap (e.g., for RISC-V FORTRAN, Vector pragmas, autovectorizers, OpenMP, MPI, BLAS, TensorFlow, etc.)
- Communicating ISA standards alignment for HPC (e.g., Vector and other ISA extensions for Supercomputers, 57b, 64b, 128b addressing, reproducible floating-point and/or other floating point standards (RISC-V bfloat16, POSITS) , etc.)
- Enabling current and future applications with simulation, emulation, verification and compliance testing capabilities.
- Enabling accelerators for a variety of domains (software and hardware) with well thought out interfaces, ISA extensions and other infrastructure and specifications.
- Engaging with physical design and foundries to facilitate implementation with new and existing technologies and IP.

Some SIG-HPC RISC-V Business Topics

- Engage and represent RISC-V in compute intensive industry and academic events, including HPC, AI/ML/DL, and embedded domains.
- Identify key industrial and academic partners with aligned interest around a common set of features for high performance, low power systems. This would enable repurposing of the hardware across many application/software domains.
- Navigating international political and legal requirements and restrictions
- Support global technology independence with a RISC-V ecosystem roadmap and partners.

What's Next??

- So many options what do I use??
  - Cores
  - Accelerators
  - NoC, Coherence, …, Oh My!!
- Independent of ISA
  - CI/CD flows
  - Development Language
  - Coding style and methods
  - Best practices for design, verification, CAD, PD, etc.
  - Enable R&D (with IP/infrastructure) and not build new wheels…
- **Find/Reuse of common components/use cases…**



Break Out Meetings Starting Now

- Opening up the rooms for chatting with the speakers.

- Thank you and continue the work and conversations!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Thank you