Microwatt and GHDL - An Open Hardware CPU written in VHDL, synthesized with Open Source tools

—

Anton Blanchard IBM

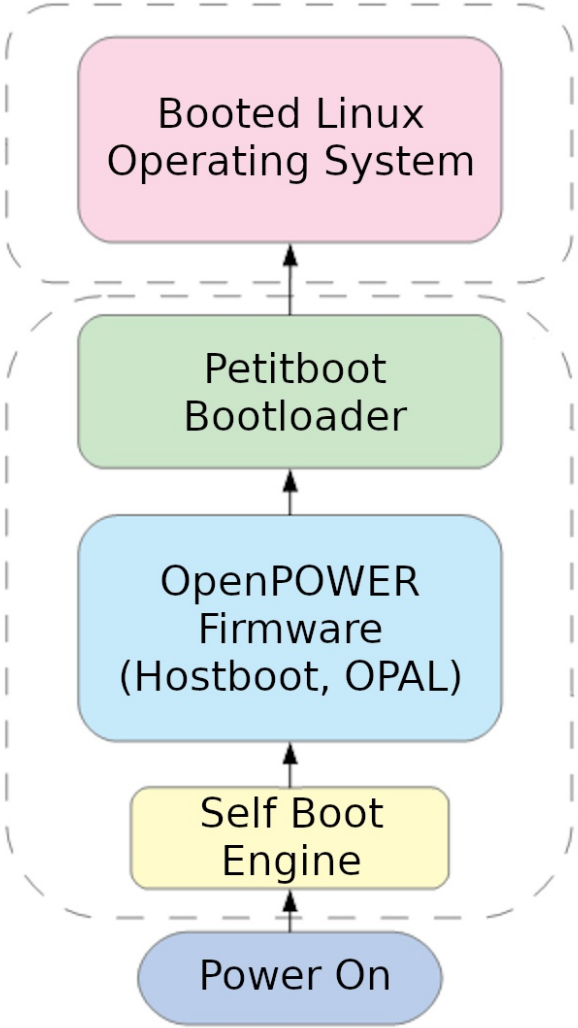
Power

summit
IBM

OpenPOWER™

Open Source Firmware

Entire firmware stack is Open Source and available on github



Raptor POWER9 Workstation

Provides a native development environment

Uses the same Open Source firmware stack

THENEXTPLATFORM

BIG BLUE OPEN SOURCES POWER CHIP INSTRUCTION SET

August 20, 2019 Timothy Prickett Morgan

POWER OpenISA Announced in August

The POWER Instruction Set Architecture is now open

Royalty free, inclusive of patents

OpenPOWER Foundation moves under the Linux Foundation

Also released a reference implementation called Microwatt

Microwatt

Tiny POWER core

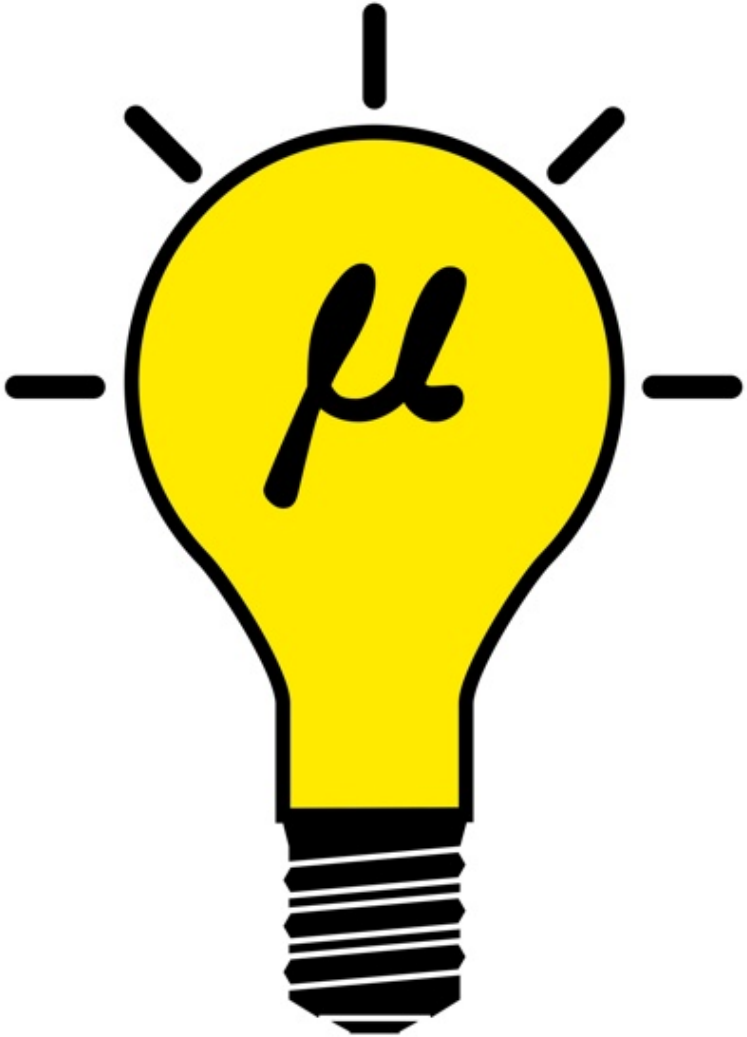
Open ISA scalar subset

Written in VHDL 2008

ghdl Open Source simulation

ghdl/yosys/nextpnr Open Source synthesis

https://github.com/antonblanchard/microwatt



Microwatt

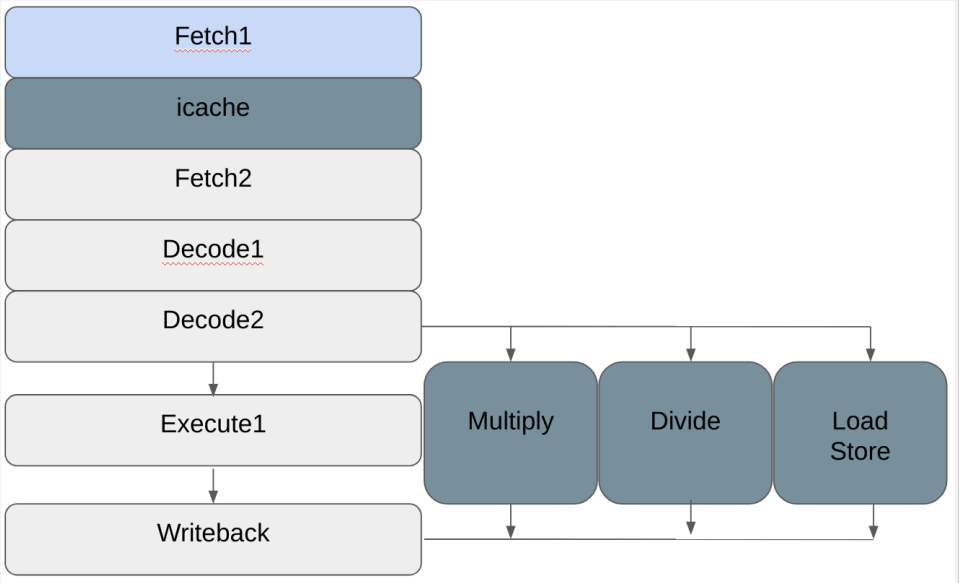
Single issue

In order

Aims to be simple and easy to understand

Reuse from the Open Hardware world

- UART, DRAM, Ethernet



antonblanchard / **microwatt**

Watch 25 | Star 307 | Fork 53

Code | Issues 10 | Pull requests 6 | Actions | Projects | Security | Insights

Branch: master | Go to file | Clone

mikey committed cc27e23 1 hour ago ✓ — **676** commits | **5** branches | **0** tags

.github/workflows	Move from travis to github workflow	18 days ago
constraints	Initial support for ghdl synthesis	5 months ago
fpga	spi: Fix dat_i_l constraints	6 days ago
hello_world	Makefile: Improve clean a bit	2 months ago
include	xics: Add simple ICS	10 days ago
lib	sw: Properly mask syscon register fields	19 days ago
litedram	Fix ld error in elf maketarget	3 days ago
media	Add title image	9 months ago
micropython	Update micropython	5 months ago
openocd	flash-arty: update error message (**#203**)	16 days ago
rust_lib_demo	console: Move console files	2 months ago
scripts	Add core logging	16 days ago
sim-unisim	Add a debug (DMI) bus and a JTAG interface to it on Xilinx FPGAs	9 months ago

About

A tiny Open POWER ISA softcore written in VHDL 2008

vhdl | processor | openpower | ppc64le

Readme

View license

Releases

No releases published

Contributors 16

+ 5 contributors

Language support

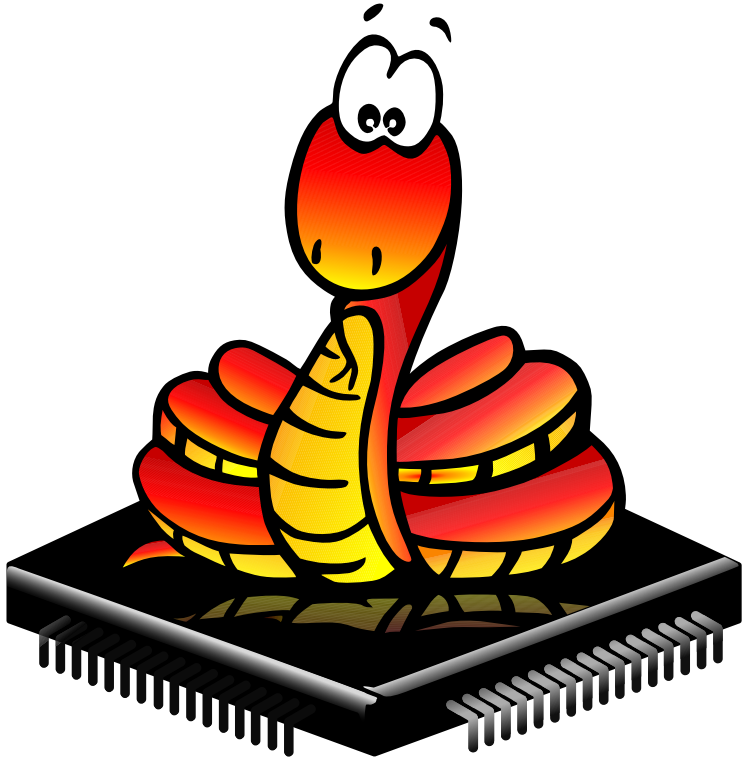
We’ve been able to leverage the strength of the PowerPC ecosystem

Lots of stuff “just works”

- I use a distro toolchain for my development work

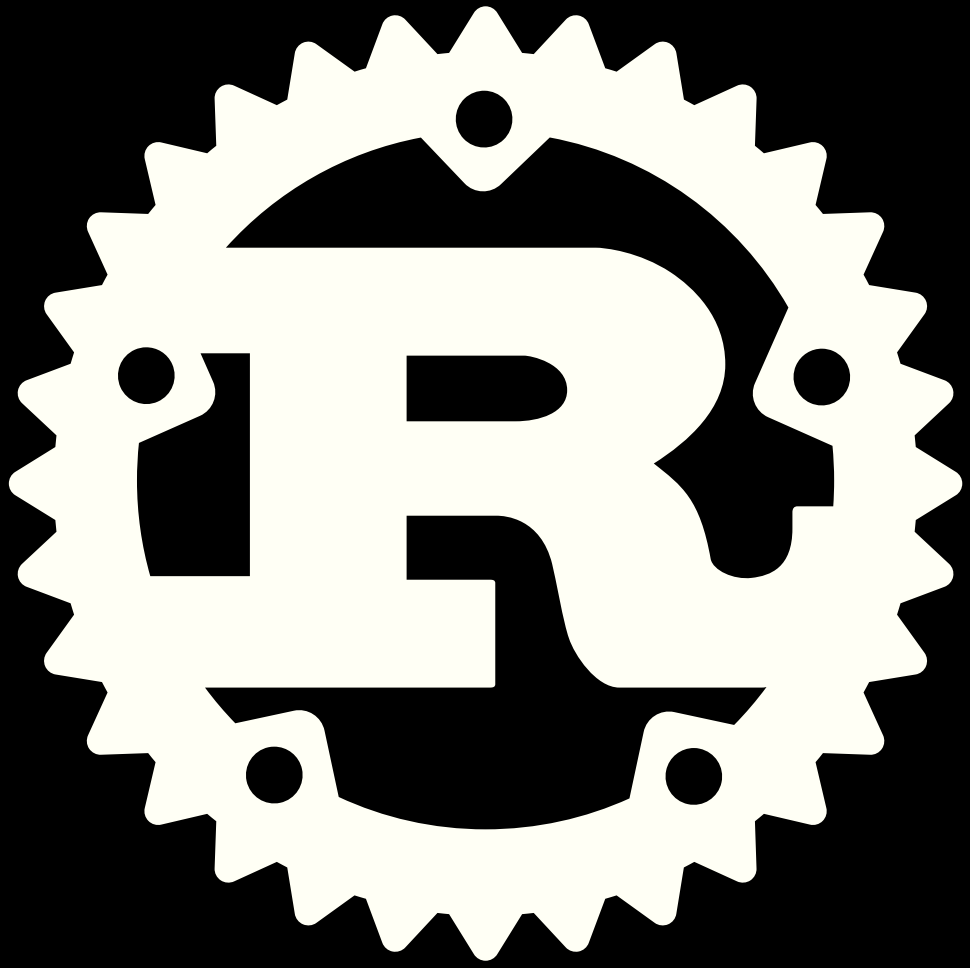
We have been adding platform support for key languages

- Thanks to Michael Neuling, Jordan Niethe, Tom Vijlbrief and Paul Mackerras.



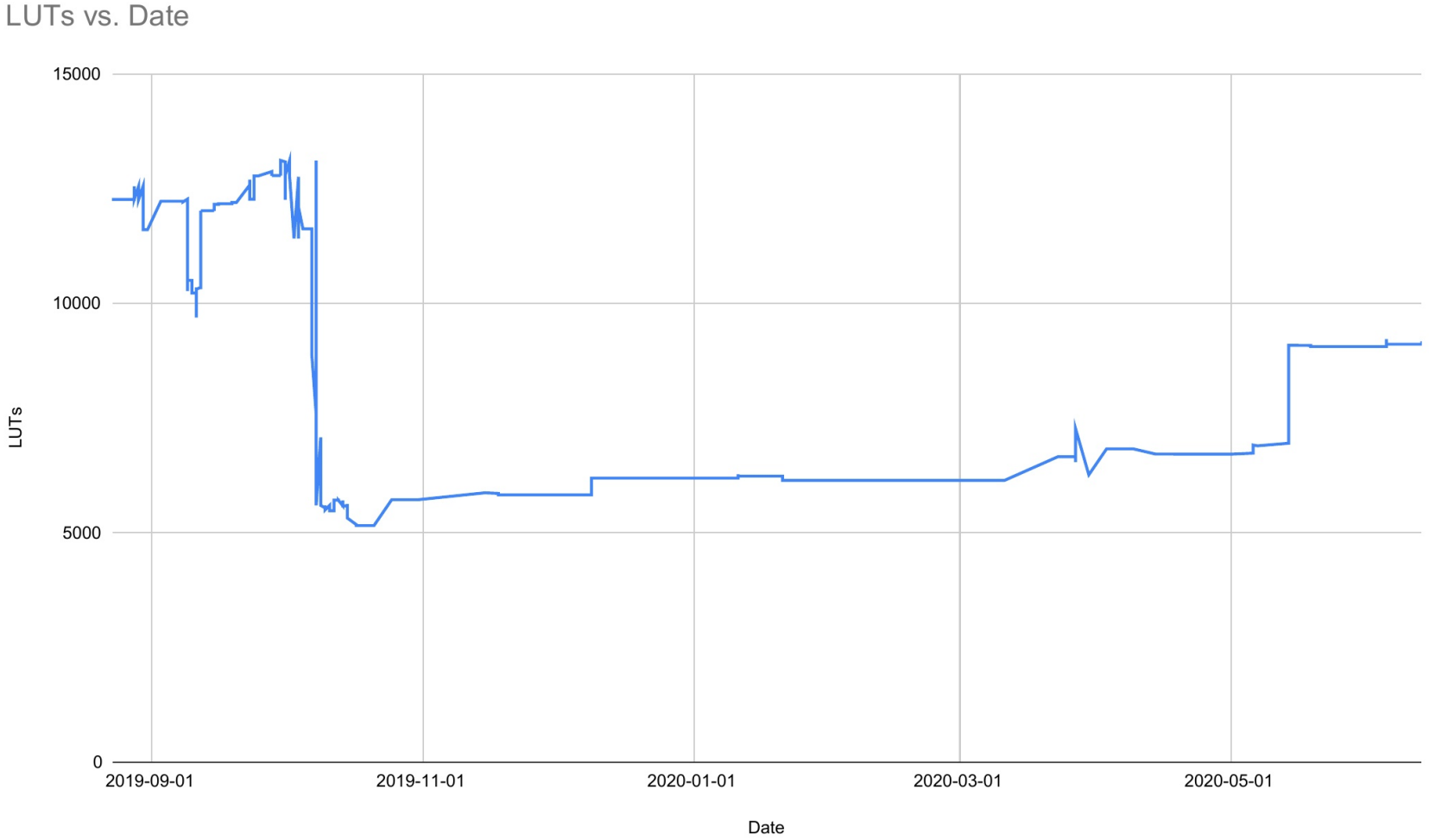
MicroPython

Zephyr™



pforth

Linux


LUTs vs. Date
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2019-11-01
2020-01-01
2020-03-01
2020-05-01
Date

Recent Developments

LiteX (DRAM, Ethernet) - Ben Herrenschmidt and Florent Kermarrec

Icache/dcache – Ben Herrenschmidt

Branch predictor – Paul Mackerras

Interrupts – Michael Neuling and Ben Herrenschmidt

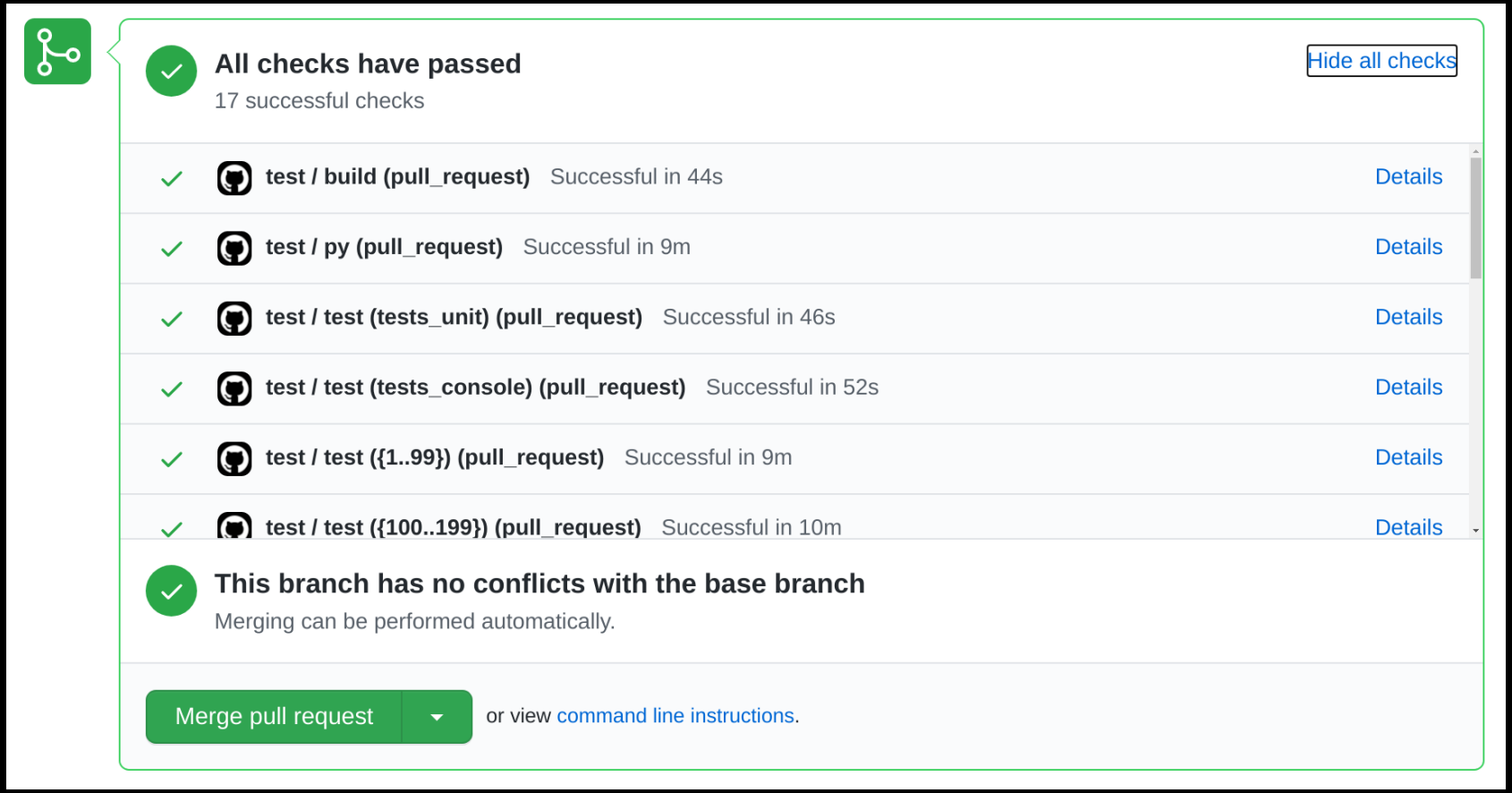
TLB – Paul Mackerras

Linux – Paul Mackerras

Continuous Integration – Michael Neuling

Many community contributions (215 github commits)

Continuous Integration



Hardware Reuse

Microwatt implements the Wishbone bus

- Simple, open protocol, widely used in the Open Hardware world
- Allowed us to interface with LiteX project
  - DRAM, Ethernet
  - More to come

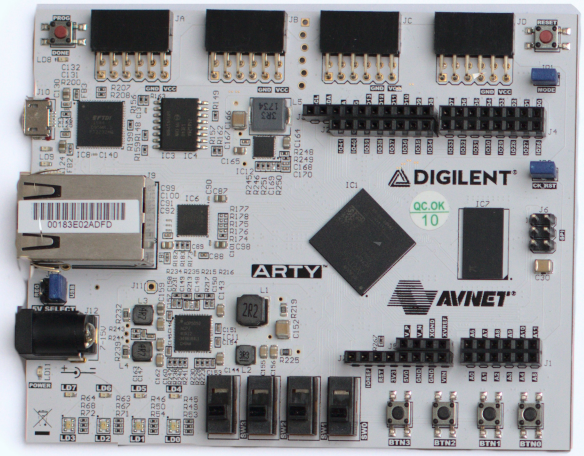
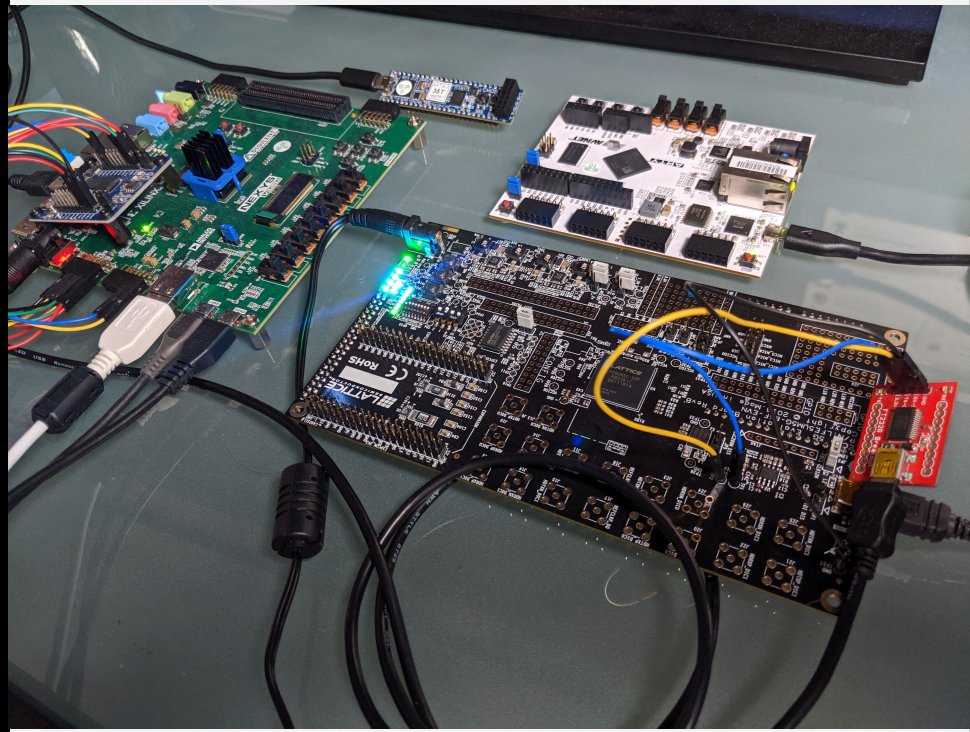
Open Source Simulation and Synthesis

Simulation done using GHDL

- Great environment for testing, including CI
- Good language support, including VHDL 2008
- Maintainer is very responsive!

GHDL recently added synthesis support

- Allows completely Open Source flow for FPGA synthesis
- Also allows VHDL → Verilog conversion via yosys, and mixed language simulation and synthesis.


DIGILENT
ARTY
AVNET
XILINX
NEXYS
VIDEO
ANALOG DEVICES

Come join us!